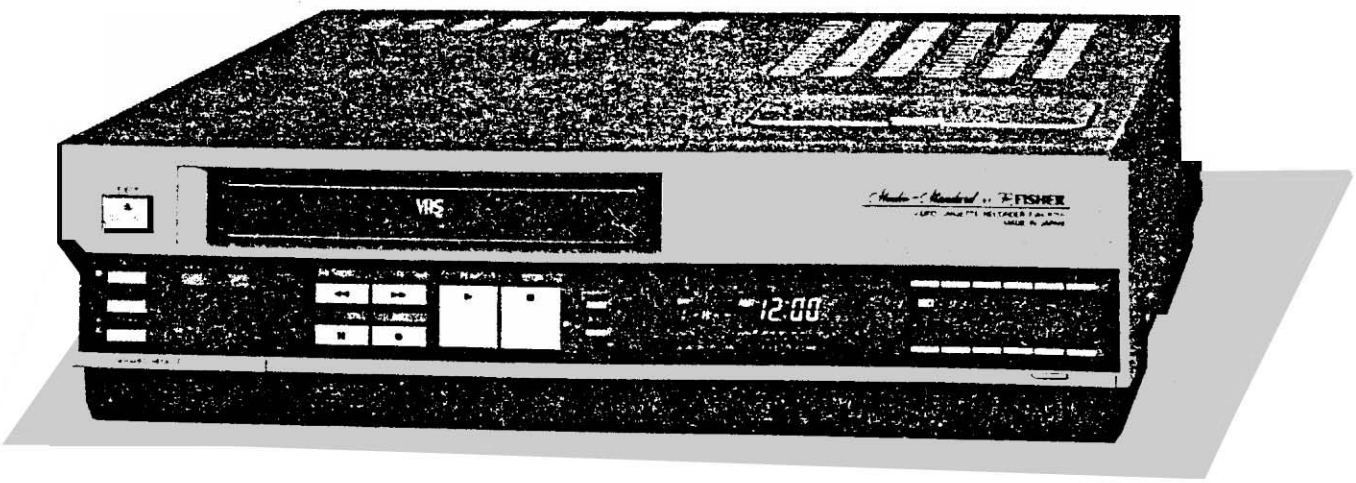
ORDER NO. VRD9001M103

Service Manual

Video Cassette Recorder

FISHER VHS HQ
PAL

FVH-P715



FISHER

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1. SPECIFICATIONS

General Specifications

Television system	PAL standard colour (system B & G) & CCIR monochrome signals 625 lines
Recording system	Rotary two-head helical scan system.
Format	VHS PAL standard
Tape width	12.7mm
Tape speed	22.39mm/sec.
Recording time	240 minutes with E-240 cassette
Tape loading system	Automatic loading
Tuner channel selection system	Soft touch, 12 preset channels
Tuner channels	UHF: # 21 - # 69
RF Converter output	UHF channel 37 (30 - 39 adjustable)
Time indication	AM/PM 12-hour display system
Timer	9-days 1 programme
Tape counter	Separate 4-digit electronic display
Auto rewind system	Activated at end of the tape when FUNCTION ON switch is pressed
Terminals	
Aerial input	DIN (socket)
RF output	DIN (plug)
Video input/output	BNC connector
Audio input/output	RCA connector
Camera remote pause	2.5mm jack

Electrical Specifications

Video output level	1 Vp-p
Video output impedance	75 ohm
Audio output level	−6.dB
Audio output impedance	600 ohm
Video input level	0.5 - 2.0 Vp-p
Video input impedance	75 ohm
Audio input level	−20 dB
Audio input impedance	50 kohm
Video S/N ratio	43 dB
Audio S/N ratio	42 dB
Audio bandwidth	50 Hz - 10 kHz
Horizontal Resolution	Colour 240 lines

Other specifications

Power requirement	240V, 50 Hz
Power consumption	36 Watts
Dimensions	440 mm(W) x 117 mm(H) x 365 mm(D)
Weight	10 kg (Approximate)

Because its products are subject to continuous improvement, Fisher Corporation reserves the right to modify product designs and specifications without notice and without incurring any obligation.

2. CIRCUIT DESCRIPTION

2-1. VIDEO CIRCUIT

2-1-1. GENERAL

The VHS system achieves very low tape consumption and uses low cost video cassette tape. Recording time in the standard play mode has become 4 hours.

Increased recording time results from the narrow gap video heads, high sensitivity video tape and the slant azimuth recording head configuration which eliminates the need for a guard band between recorded tracks. In addition, the VHS format takes into consideration special operating modes such as still picture, slow motion and speed playback.

Adoption of the VHS format presented several technical challenges. Foremost among these were obtaining high picture quality and high resolution despite the slow (4.9 meters per second) relative speed between the tape and video heads, improving signal to noise ratio (S/N), and preventing black to white reversal phenomena due to the short recording wavelength of 1.0μm. Also the $\pm$6° azimuth angle of the video heads alone is not sufficient to eliminate crosstalk from the down converted color signal.

Steps for solving these difficulties included adoption of a nonlinear emphasis circuit and selecting the emphasis amount for optimum S/N. The reversal problem was overcome by using a noise canceller circuit, while a phase shift system has been designed for eliminating color crosstalk.

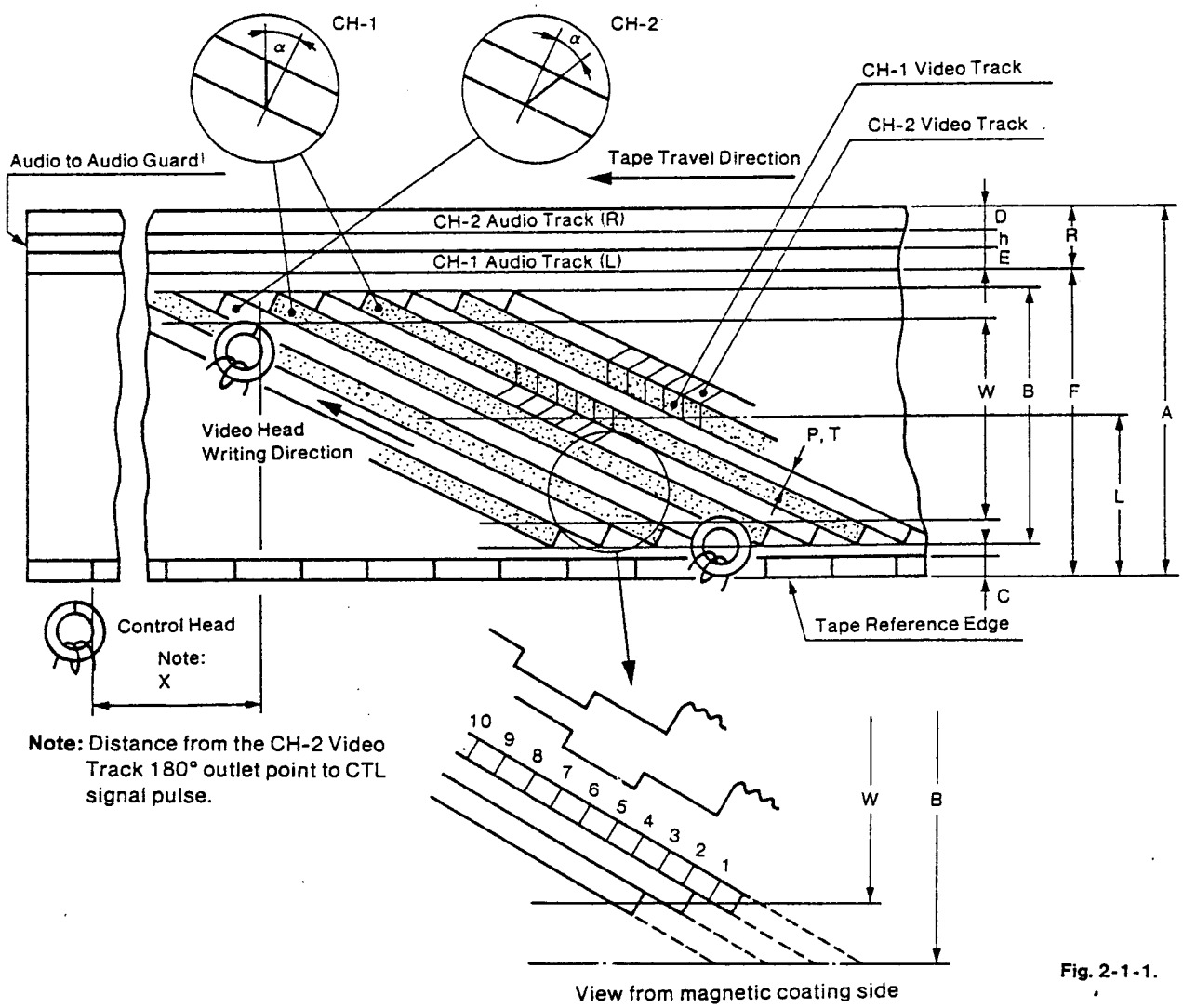
The following discussion covers several main points of the VHS format.

2-1-2. MAGNETIC TAPE PATTERN

1. STANDARD

In the VHS format, two rotating video heads at $\pm$6° azimuth angle are used for recording without a guard band.

Fig. 2-1-1 indicates the recording pattern, while the pertinent values are listed in Table 2-1-1.



Note: Distance from the CH-2 Video Track 180° outlet point to CTL signal pulse.

Fig. 2-1-1.

Items			Standard	Remarks
1. (A)	Tape Width	mm	12.65 ±0.01	
2. (Vt)	Tape Speed	mm/sec	23.39 ±0.5%	
3. (ϕ)	Drum Diameter	mm	62 ±0.01	(Upper Drum)
4. (Vh)	Writing Speed	m/sec	4.85	
5. (P)	Video Track Pitch	mm	0.049	
6. (B)	Video Width	mm	10.60	
7. (W)	Video Effective Width	mm	10.07	
8. (L)	Video Track Center	mm	6.2	Measured from reference edge
9. (V)	Video Track Width	mm	0.049	
10. (C)	Control Track Width	mm	0.75	
11. (R)	Audio Track Width	mm	1.0	Single track
12. (D)	Audio Track Width	mm	0.35	CH-2 (R)
13. (E)	Audio Track Width	mm	0.35	CH-1 (L)
14. (F)	Audio Track Reference Line	mm	11.65	Measured from reference edge
15. (h)	Audio to Audio Guard Width	mm	0.3	
16. (θo)	Video Track Angle		5°56'7.4"	(Stopped)
17. (θ)	Video Track Angle		5°57'50.3"	(Running)
18. (α)	Video Head Gap Azimuth Angle		6° ±10'	
19. (X)	Positions of Audio and Control head	mm	79.244	
20. ( )	Positions of Front Edge of V-SYNC		5 ~ 8H	Inside the W bottom edge
21. ( )	Tape Back-Tension		30 ~ 45g	At tape beginning and at the drum entrance

Table 2-1-1 Magnetic tape pattern

Note: Tests and measurements shall be made under the following conditions.
Temperature: 20°C ±2°C, Relative humidity: 65% ±5%

2. HORIZONTAL CORRELATION

The azimuth head configuration removes crosstalk from most of the high frequency portion of the FM luminance signal, however, it is not able to fully eliminate crosstalk from the low frequency component of the lower sideband portion. This residual crosstalk is reduced by employing line correlation for the tape pattern.
Line correlation (or "H correlation") consists of arranging the horizontal sync signal positions of adjacent recorded tracks. Since this makes the frequencies of the main signal and crosstalk signal very close, the demodulated crosstalk amount becomes extremely low with respect to the main signal. The type of H correlation used in the VHS format is shown in Fig. 2-1-2.
In order to provide H correlation in the tape pattern, tape speed, head drum diameter and other factors must be decided. The adjacent track correlation in the VHS format is 1.5 H. This 1.5 H difference is important not only for removing low frequency crosstalk from the luminance signal, but also for correcting color signal crosstalk in the SECAM system, for which phase shifting cannot be used.

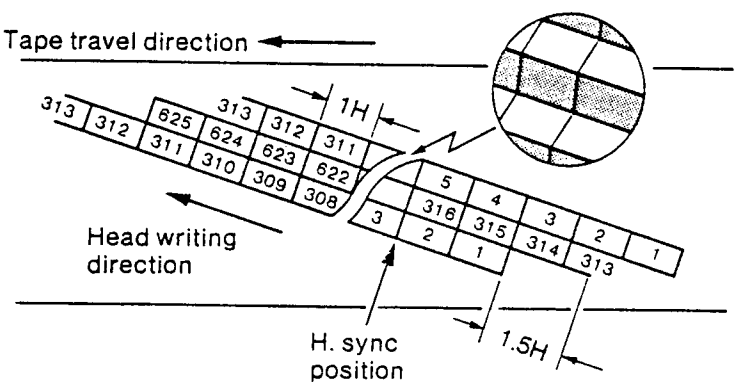


Fig. 2-1-2.

2-1-3. LUMINANCE SIGNAL RECORDING SYSTEM

1. GENERAL

Frequency modulation (FM) is used for the luminance signal recording system. A simplified block diagram of the system is shown in Fig. 2-1-3.

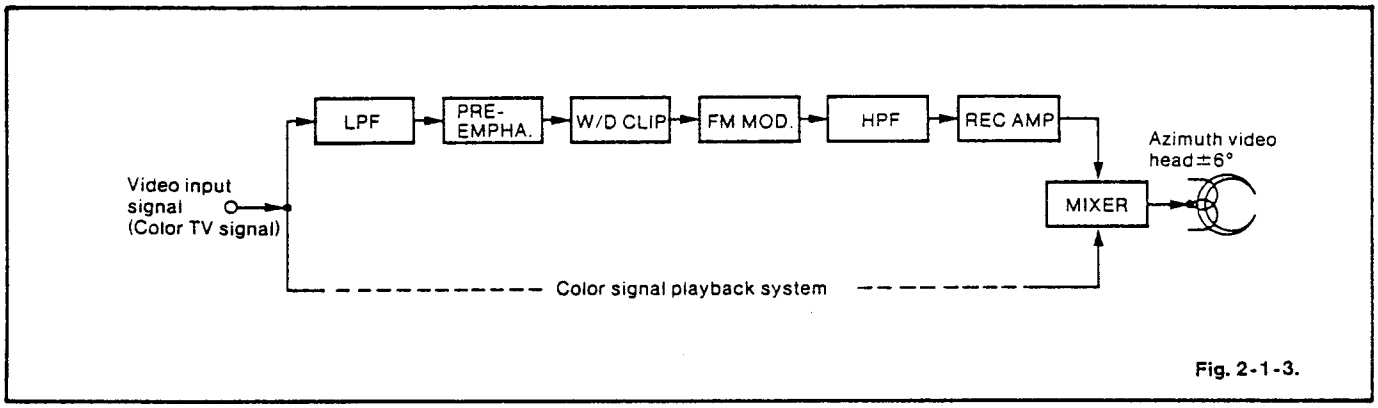


Fig. 2-1-3.

A lowpass filter (LPF) removes the color component and passes only the luminance component of the input color TV signal. At the next stage pre-emphasis circuit, the high frequency portion of the luminance signal is enhanced in order to improve S/N during FM recording. Since excess pre-emphasis could lead to black/white reversal due to the shortened recording wavelength, a white/dark clip circuit cuts the overshoot and undershoot components which exceed certain positive and negative levels.

The frequency modulator (FM MOD) converts the AM luminance signal to FM, which goes through a highpass filter (HPF) to the recording amplifier. These circuits amplify the signal with the proper frequency characteristic, after which it is mixed with the down converted color signal and supplied to the video heads.
The following describes luminance signal recording and playback processes (see Figure 2-1-4). The upper section in Fig. 2-1-4 shows luminance signal path in recording mode and lower section shows playback mode.

2. INPUT SIGNAL SELECTOR CIRCUIT

The video signal is either from the tuner or the rear VIDEO IN jack. One out of these two video signal sources is selected by a relay, which is controlled with the TU-EXT switch.

The selected video signal is supplied to both the luminance and chrominance circuits.

3. ELECTRIC ELECTRIC (E-E) CIRCUIT

The E-E circuit allows the user to monitor the signal being recorded at the Line Out jack or to view TV programs using the VTR tuner.

The video signal is supplied to pin 26 of IC202 (luminance circuit), where the signal is amplified through an AGC and E-E amplifiers, then output to pin 5. The signal then goes to a switching transistor (Q258) which selects only the E-E and REC modes, after passign through an emitter follower (Q257). The output of the switching transistor is input to RF converter via an emitter follower (Q242) and RF delay equalizer (L289).

The video signal branched at Q242 is applied to the rear VIDEO OUT jack via an emitter follower (Q244).
The RF converter converts the video signal into a TV signal whose frequency corresponds channels 30 through 39.

The signal being recorded can be monitored at either the RF OUT or Line Out jack using the appropriate monitor.

4. AGC CIRCUIT AND 3.5MHz LOW-PASS FILTER (LPF)

The output of the AGC amplifier within IC202 appears at pin 24 of the IC. This output goes to a 3.5MHz LPF (L286) and delay equalizer (L285) via emitter follower (Q234, Q232).
The 3.5MHz LPF separates the video signal into the luminance and chrominance signals. The LPF characteristics are shown in Figure 2-1-6.

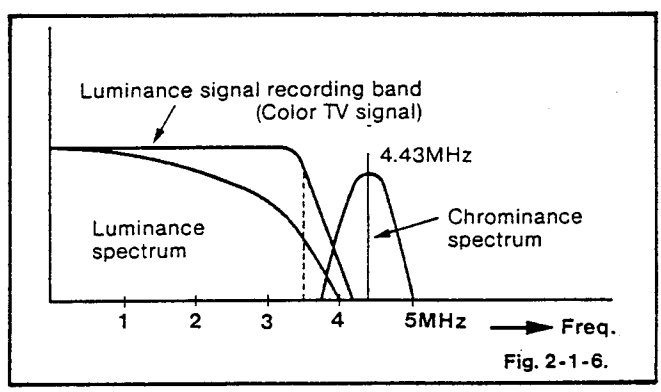


Fig. 2-1-6.

The output of the LPF is input to pin 13 of IC202, where the luminance signal is amplified by an internal video amplifier to compensate for the loss caused by the LPF and equalizer. The luminance signal appearing at pin 14 of IC202 branches to a clamp circuit (pin 18 of IC201), sync separation circuit (pin 1 of IC202), and AGC circuit (pin 28 of IC202).

Luminance Signal Block Diagram

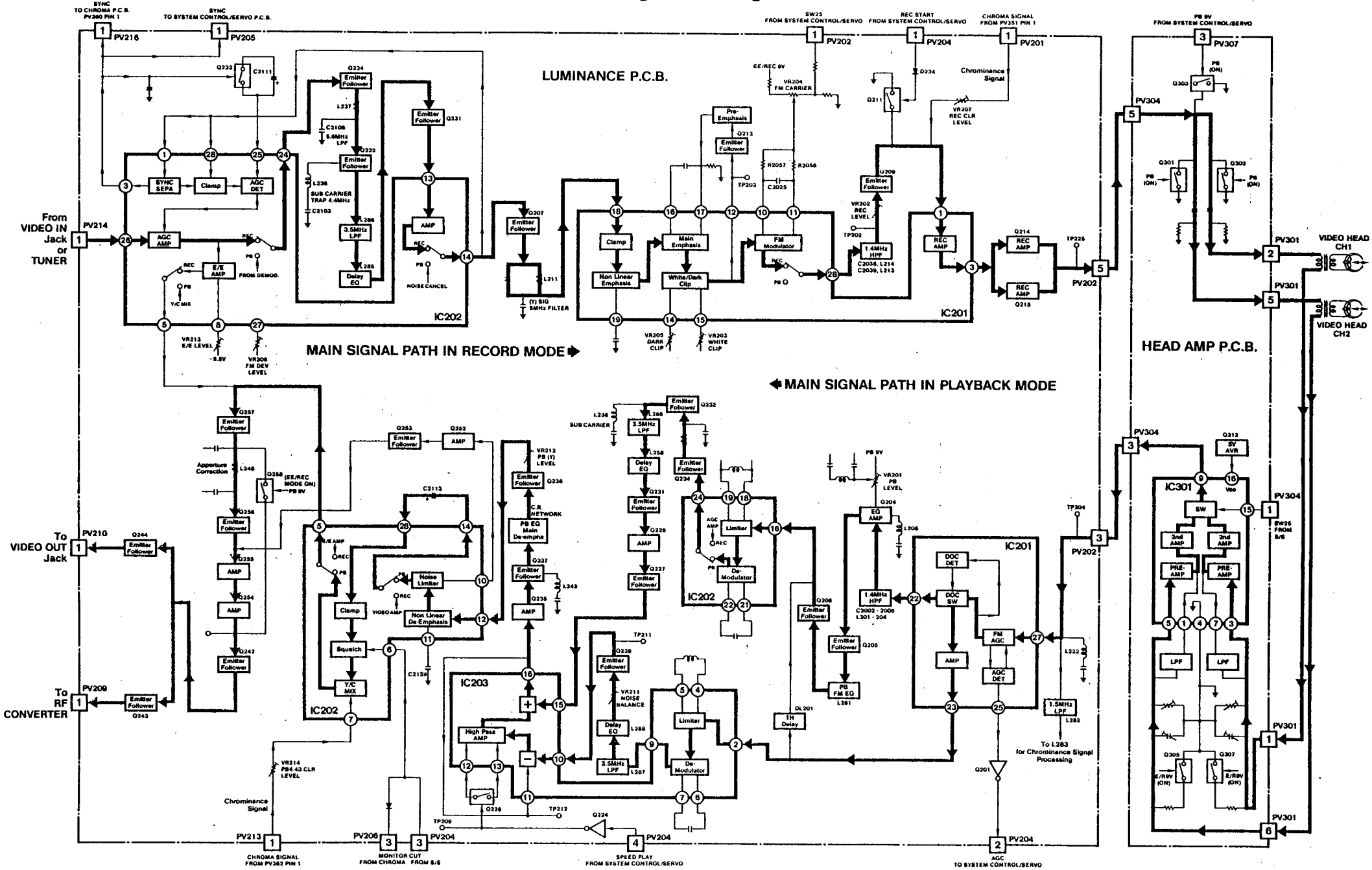


Fig. 2-1-4.

Chrominance Signal Block Diagram

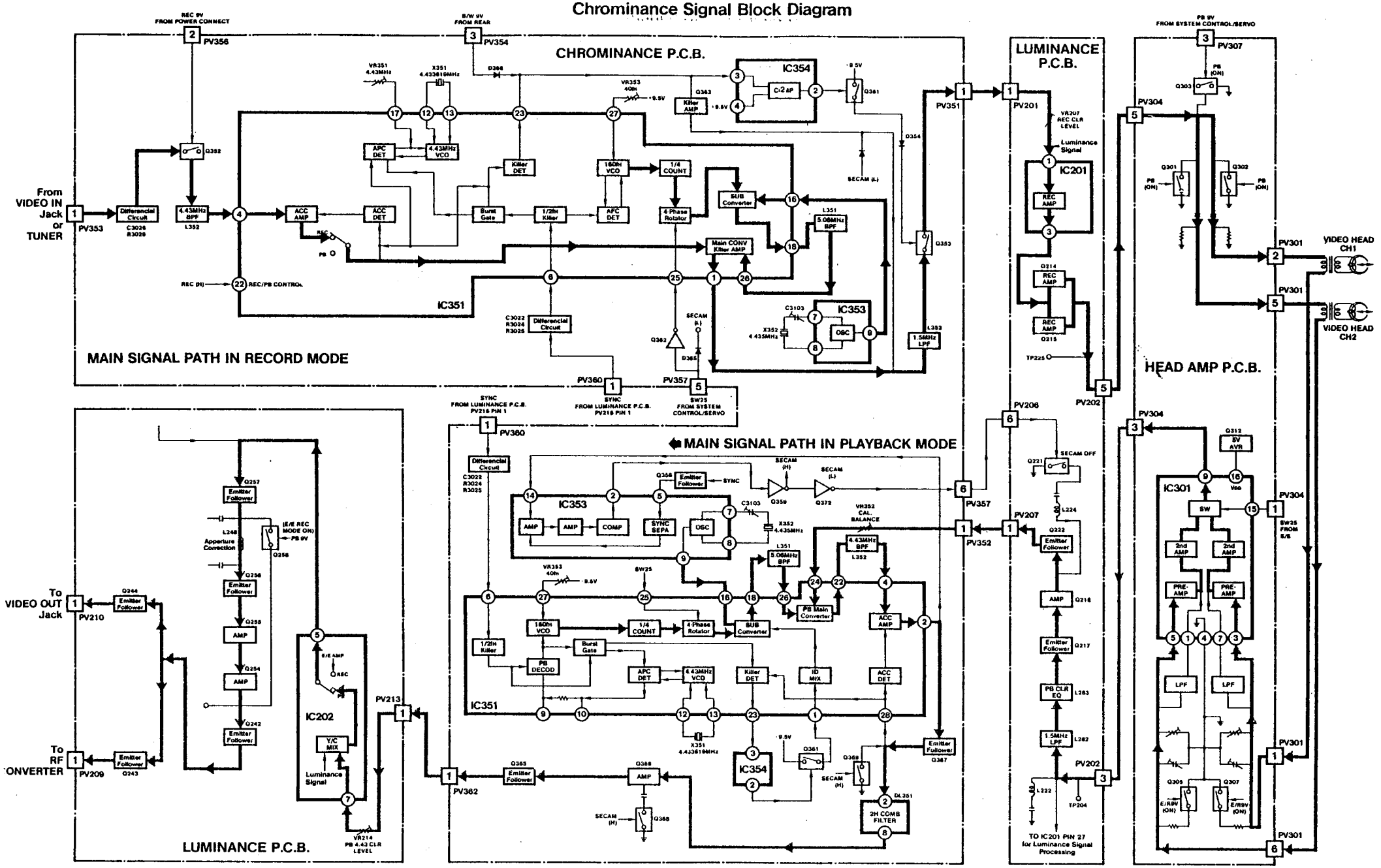


Fig. 2-1-5.

The AGC and sync separation circuits provide the video signal with AGC control. The following describes AGC operations;
The typical ratio of signal levels of the sync signal to the luminance signal (both contained in the video signal) is 3:7. The sync signal contained in the input signal is, however, not constant in its level, and the luminance signal level also varies with the picture brightness.
The sync AGC circuit detects the amplitude of the sync signal level and regulates it to a constant level.
The sync AGC circuit, when the sync signal level is low, increases it, which also increases the luminance signal level. If the luminance signal level is saturated, the picture will loose contrast, with color balance leaned to white, however. To prevent this, the sync AGC functions as a peak AGC when the sync ratio is less than 26.7% (with respect to the luminance signal), so as to regulate the video signal to a constant level.
Figure 2-1-7 shows sync signal ratio versus video signal. If we sassume that the sync signal ratio is 50%, or in other words, the luminance signal is at 30% (gray level) with respect to its peak level, the sync signal component is 0.3 Vp-p and the luminance signal component is 0.3 Vp-p. This provides for an AGC output level of 0.6 Vp-p for the video signal.

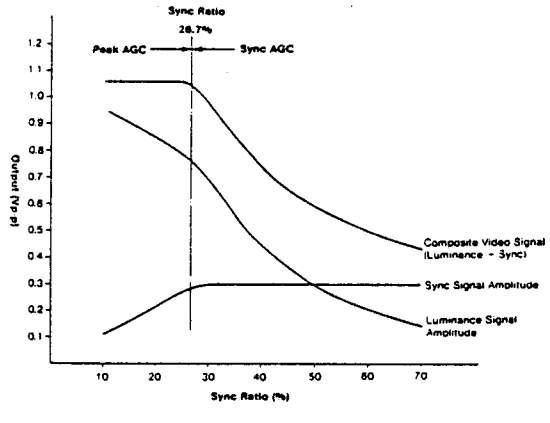


Fig. 2-1-7.

The AGC circuit used in this VTR covers a video signal level range of 0.5 to 2 Vp-p to provide a constant video output of 1 Vp-p.

5. CLAMP CIRCUIT

The luminance component of the video signal varies with the brightness (APL) of the picture (Figure 2-1-8(a)).
When the signal is passed through capacitor coupling circuit, its DC component is blocked by the capacitor, resulting in irregular tip levels of the sync signal (Figure 2-1-8(b)). The clamp circuit is used to align the lower limit of the modulation frequency to the sync tip level in the following FM modulator.
The clamp circuit is contained in IC201, whose pin 18 presents a clamped waveform (Figure 2-1-8(c)).

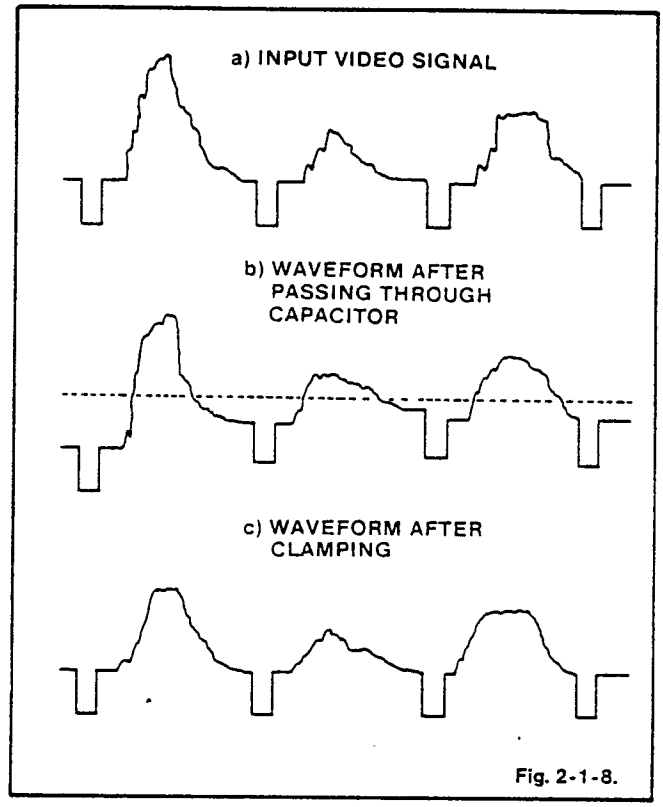


Fig. 2-1-8.

6. EMPHASIS CIRCUIT

In FM modulation-demodulation system, demodulation noise linearly increases according to modulation signal level. This results in reduced signal-to-noise ratio in high frequency range.
To improve the S/N ratio, the signal level in high frequency range is emphasized beforehand during recording.
This method is called pre-emphasis. The pre-emphasis is composed of non-linear emphasis and main emphasis.
A low-level luminance signal has a lower S/N ratio than a high-level luminance signal. To compensate for this, the non-linear pre-emphasis technique is used, in which emphasis is increased for low-level input and reduced for high-level input. The emphasis characteristic is controlled by the capacitor connected to pin 19 of IC201.
Figure 2-1-9 shows a non-linear emphasis characteristic.

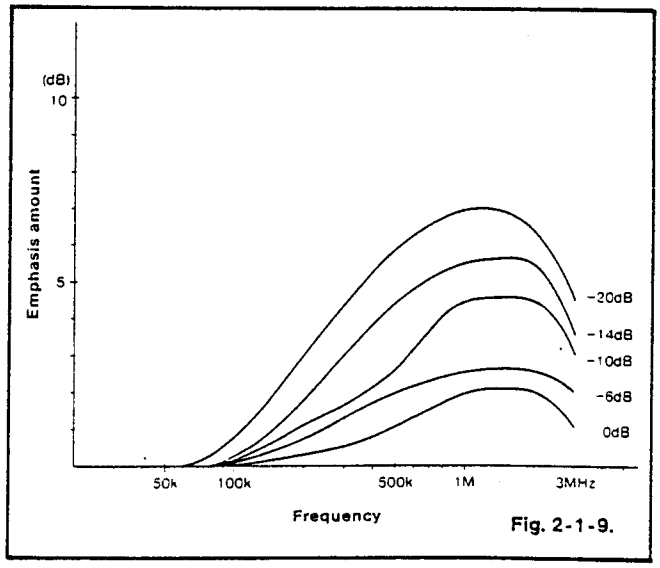


Fig. 2-1-9.

The main emphasis circuit emphasizes the high frequency spectrum independent of the signal level. The luminance signal is fed back from pin 12 of IC201 to pin 17 via Q213 and C.R. circuit which provides the emphasis frequency characteristic. The main-emphasis characteristic is shown in Fig. 2-1-10.

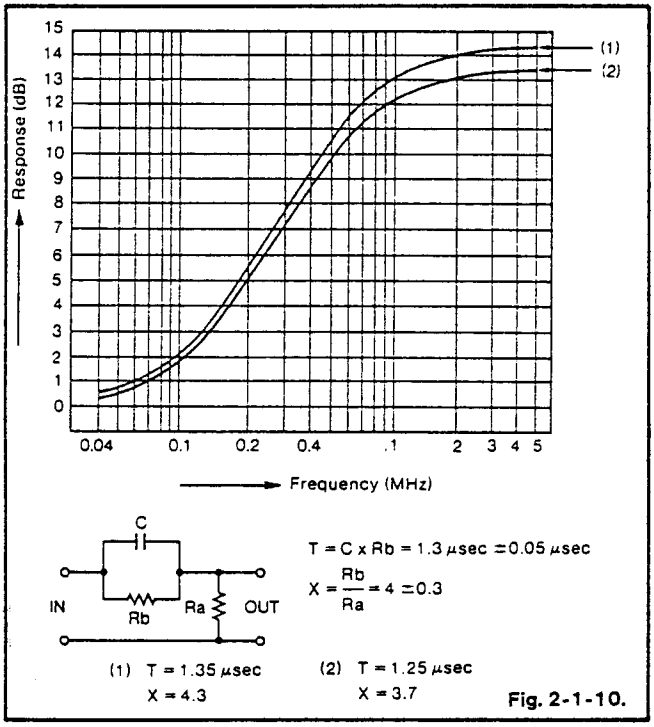


Fig. 2-1-10.

7. FM MODULATOR

After going through the pre-emphasis, white clip, and dark clip circuits, the luminance signal is input to an FM modulator, where it is modulated into an FM signal.

The FM modulator uses an astable multivibrator, whose time constant is determined by capacitor C2025 (120 PF) and resistors R2056 (6.8 kΩ) and R2057 (6.8 kΩ).

The FM carrier frequency is controlled with VR204 to set the sync tip to 3.8MHz.

The luminance signal level is controlled with VR209 connected to pin 27 of IC202, so that the white peak is at 4.8MHz to achieve the specified frequency deviation.

Figure 2-1-11 shows a relationship of the luminance signal with FM frequency.

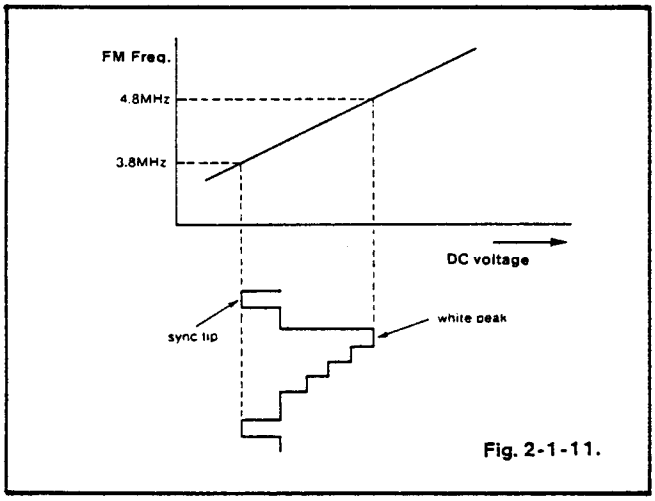


Fig. 2-1-11.

8. WHITE AND DARK CLIP CIRCUIT

The luminance signal, after passing through the pre-emphasis circuit, produces sharp overshoot and undershoot at the leading and trailing edges as shown in Figure 2-1-12 because its high frequencies is emphasized. If this signal is directly modulated, the overshoot or undershoot will cause an overmodulation, which will result in a reverse video at the boundary of black and white on the demodulated picture.

On the other hand, a reduced overshoot or undershoot causes reduction of resolution. As a compromise, the VHS standard specifies an overshoot/undershoot clipping level.

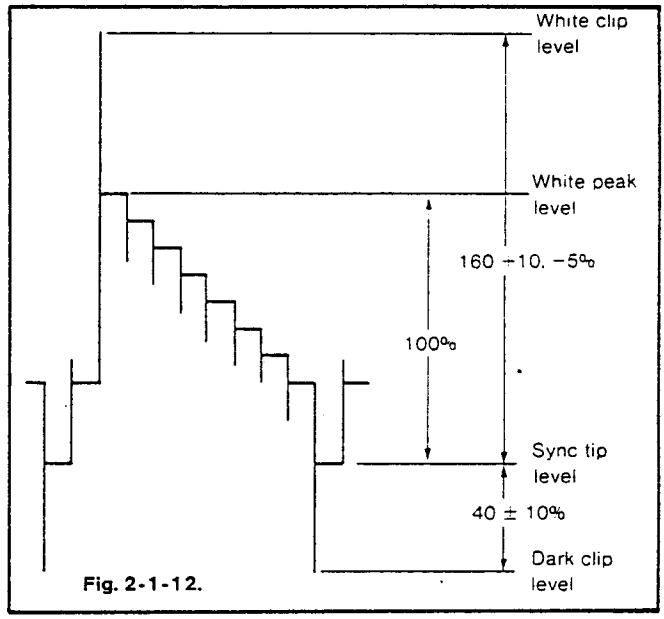


Fig. 2-1-12.

9. 1.4MHz HIGH PASS FILTER (HPF)

After FM modulated, the luminance signal output appears at pin 28 of IC201. This output goes to the HPF shown in Figure 2-1-13, where the frequency component below 1.4MHz is attenuated. This prevents beat interference between the low frequency component below 1.4MHz passed through the modulator and the down-converted chrominance signal.

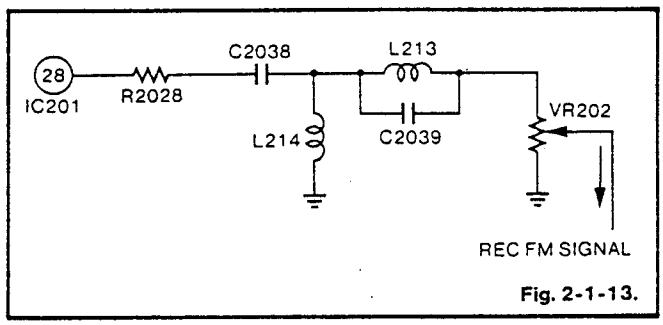


Fig. 2-1-13.

10. LUMINANCE/CHROMINANCE MIXER CIRCUIT

After passing through the 1.4MHz HPF, the FM signal is adjusted by VR202 (rec y level adjust.) to the optimum recording current via emitter follower (Q209). The luminance signal is sent to pin 1 of IC201.

In the mean time, the down-converted chrominance signal passed through the 1.5MHz LPF is adjusted by VR207 (rec C level adjust.) and then applied to pin 1 of IC201, where it is mixed with the luminance signal.

11. REC AMPLIFIER CIRCUIT

The signal is amplified by a rec amplifier within IC201 to approximately 20dB, and the output of the amplifier appears at pin 3 of the IC. The output signal is supplied to the head amplifier via an amplifier (Q214, Q215).

2-1-4. LUMINANCE SIGNAL PLAYBACK SYSTEM

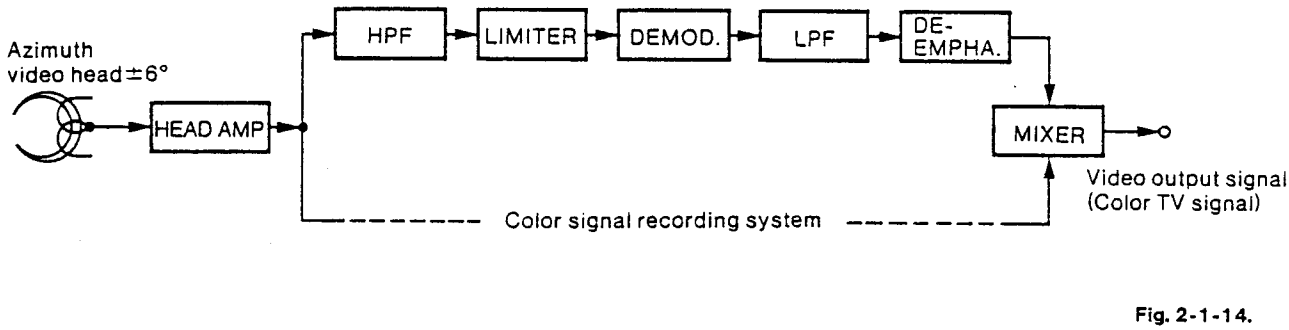


Fig. 2-1-14.

1. GENERAL

This system functions to return the signals recorded on the tape to a form as close as possible to the video input signals. The simplified block diagram is shown in Fig. 2-1-14.

The low level FM signals played back by the two video heads are combined into a single FM signal by the switching amplifier. After amplification to the required frequency characteristic, a highpass filter attenuates the down converted color signal and passes only the FM luminance signal. This HPF has the same response as that of the recording system.

Variations in the playback FM signal level due to mechanical stretching and contraction of the tape, and irregularities in tape to head contact, are corrected by the limiter circuit. The signal is amplified more than 80dB to permit precise demodulation. A double limiter circuit is employed in order to prevent black/white reversal effects.

In the following stages, the demodulator and lowpass filter return the luminance signal to its AM form. The deemphasis circuit reverses the emphasis applied during recording. From this point, the signal goes to the mixer where it is mixed with the playback color signal to become the video output signal.

The output signal from the head amp is supplied to luminance P.C.B. via PV304 pin 3.

2. PLAYBACK FM EQUALIZER

The PB FM signal from head amplifier is supplied to IC201 pin 27 via PV202 pin 3. The unevennes of playback signal is removed by the AGC circuit inside IC.
The AGC output appears at pin 22 via DOC switch circuit, and is input to 1.4MHz HPF where the down-converted chrominance signal is eliminated.

In the meantime, the AGC detector output from IC201 pin 25 is supplied to system control circuit via Q201 and PV204 pin 4. This output is used with the stop pulse signal transmitted from microprocessor inside the system control circuit to stop the capstan motor at the optimum timing to fade out the noise bar in the STILL mode.

The amplified and aligned FM signal then goes to a FM equalizer, where its frequency and phase characteristics are equalized. The equalizer restores a flat frequency characteristic for the playback output of the video head whose high and low frequency characteristics are both attenuated. The equalizer is composed of Q204, Q205, Q206 and L281.

The output of Q206 is input to pin 16 of IC202, where the FM signal is converted into an AM equivalent. The output of Q206 also branches to pin 23 of IC201 via an 1H delay line to serve as a DOC compensation signal. The output of the 1H delay line also goes to pin 2 of IC203, a noise canceller.

3. DROP-OUT COMPENSATION CIRCUIT (DOC)

A dropout of magnetic body off the tape surface or dust particle on it causes white horizontal line noise on the playback picture. This is called a dropout. In most cases, the luminance signal is missing or its level is extremely low at dropouts. The DOC circuit serves to making dropout noise inperceptible on the screen.

The DOC utilizes the line correlation principle for TV signal (i.e. the signals on scanning lines which departs 1H from each other on a TV picture are almost identical). The DOC circuit inserts the signal of 1H before into the dropout portion to make it inperceptible on the screen. The signal delayed by 1H is supplied by an 1H delay line (DL201) to pin 23 of IC201.

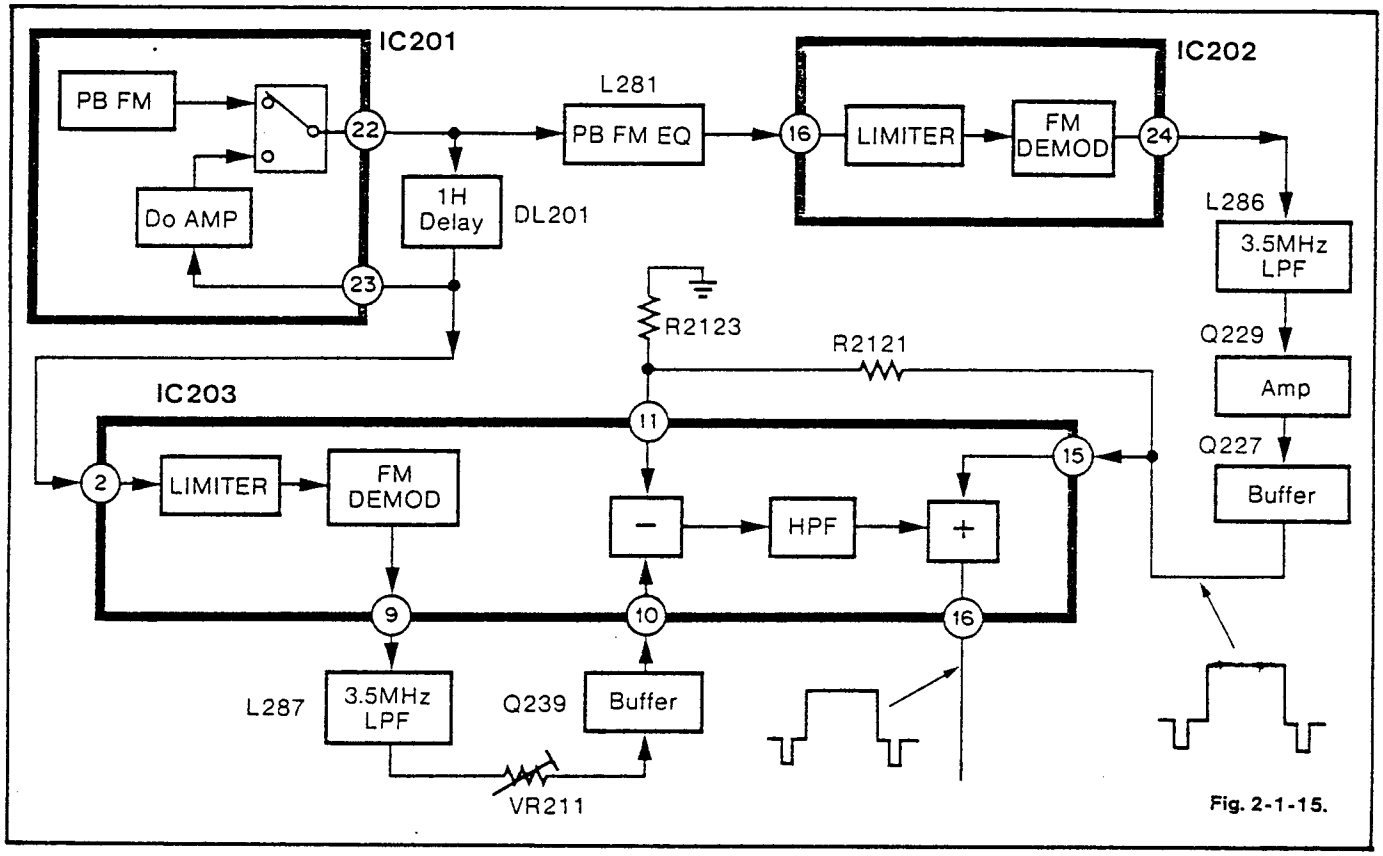


Fig. 2-1-15.

4. H CORRELATION NOISE CANCELLER

The H correlation noise canceller provides noise reduction by utilizing the line correlation principle for TV signals. When the luminance signal on the main signal line and a luminance signal with 1H delay are applied to the inputs of a differential amplifier, the amplifier provides only noise component without line correlation at its output. The noise component is added to the main luminance signal line with the phase in reverse to cancel the noise component.

The block diagram of the noise canceller is shown in Figure 2-1-14.

The main luminance signal is applied to pin 16 of IC202, where it is demodulated via a limiter. The demodulated signal goes to a 3.5MHz LPF (L286) via an emitter follower (Q234, Q232), where the luminance signal includes sync component.

The attenuated luminance signal by LPF is amplified by an amplifier (Q229), then is input to pin 15 of IC203.

The FM signal, after passing through a 1H delay line (DL201), is input to pin 2 of IC203, where it is demodulated via a limiter within the IC.

The demodulated output appears at pin 9 of IC203, and inputs to a 3.5MHz LPF (L287), where unnecessary high-range component is out off. The LPF output is applied to pin 10 of IC203.

The input signal level at pin 11 must be aligned with that at pin 10 so as to subtract the main signal from the 1H delayed signal. This alignment can be done with VR211. The noise component is reversed in its phase, and is added to the main luminance signal from pin 15. The noise-free luminance signal appears at pin 16 of IC203.

5. MAIN DE-EMPHASIS AND NONLINEAR DE-EMPHASIS CIRCUITS

The luminance signal appearing at pin 16 of IC203 is applied to the main de-emphasis circuit.
The main de-emphasis circuit consists of Q235, Q237, C2131, R2166, R2168, C2133, C2134, and C2215. and is used to de-emphasize the high frequency which was emphasized by main emphasis circuit during recording. The output of the main de-emphasis circuit is input to pin 12 of IC202, where the signal is nonlinear de-emphasized to restore the signal to its original condition. The signal then appears at pin 14 of IC202 after passing through a noise canceller within the IC.

6. LUMINANCE-CHROMINANCE MIXER CIRCUIT

The luminance signal appearing at pin 14 of IC202 is applied to pin 28. The chrominance signal is input to pin 7 of IC202, where it is mixed with the luminance signal in the mixer within the IC. The mixed video signal appears at pin 5 of IC202.

7. VIDEO OUTPUT CIRCUIT

The video signal appearing at pin 5 of IC202 is input to an apperature circuit via Q257, where the high frequency signal response is corrected to flat. The output of the apperature circuit is applied to an amplifier comprised of Q256, Q255, and Q254, whose output is input to Q242.
The output of Q242 is applied to the RF converter via an RF equalizer and emitter follower (Q243).
The output of Q242 also branches to the VIDEO OUT jack on the rear panel via another emitter follower (Q244).

2-1-5. COLOR SIGNAL RECORDING SYSTEM

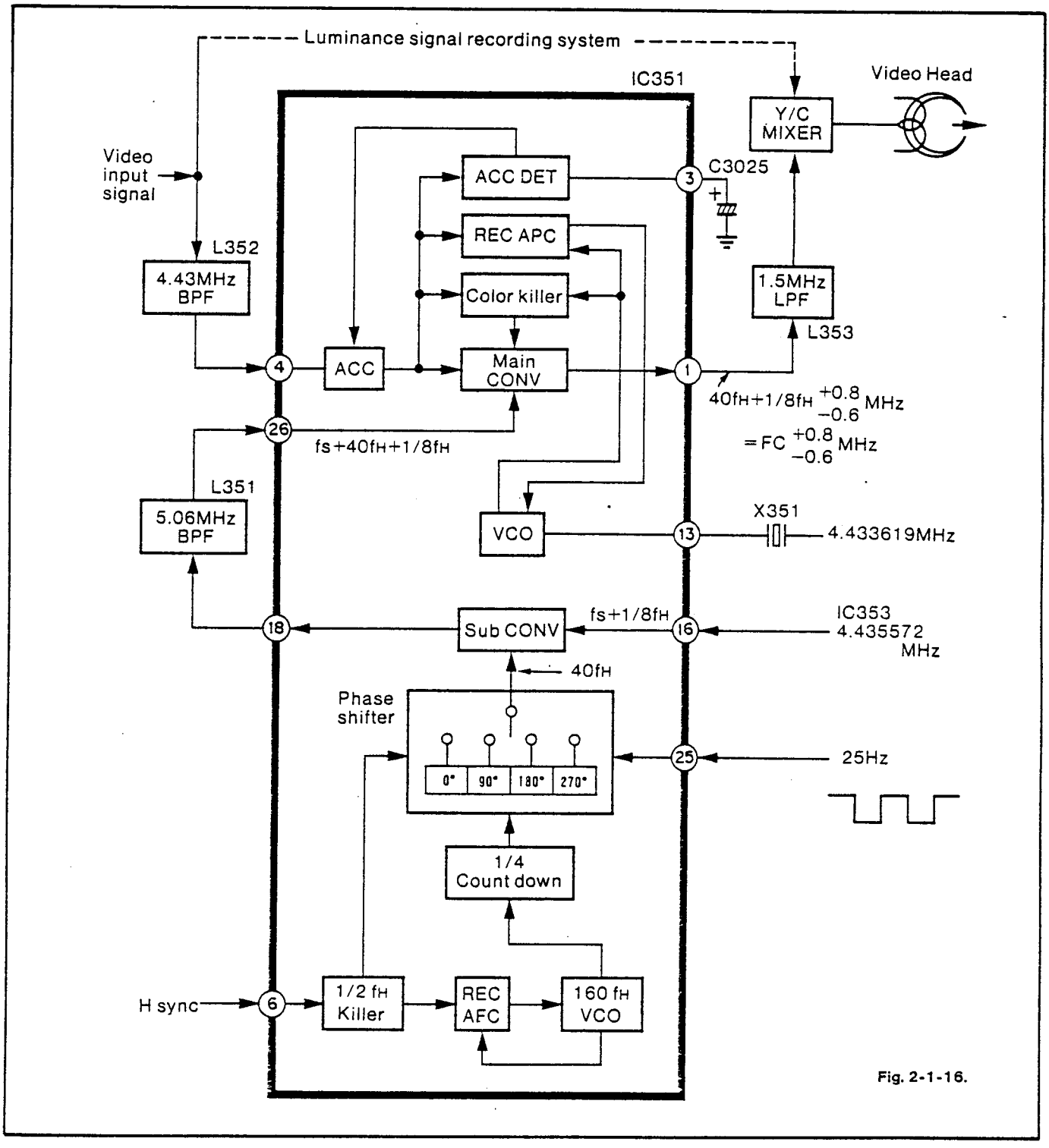


Fig. 2-1-16.

1. GENERAL

This is direct recording system using a down converted phase shifted color signal. The phase shift system removes color crosstalk which cannot be completely eliminated by the azimuth video heads. Fig. 2-1-16 illustrates a simplified block diagram of this system.

A bandpass filter (BPF) extracts the color component from the input video signal and supplies it to the main converter.

At the same time, the input signal also goes to the horizontal sync separator, which supplies the 15.625kHz (f_H) to the multiplier and phase shift circuits. Via the phase shifter, the 40 f_H CH-1 track component is supplied directly to the sub converter, but the CH-2 component is delayed in phase 90° every line (1H). A 25Hz rectangular wave synchronized to the video head rotation is used for differentiating between the CH-1 and CH-2 components. Each line is also controlled by the f_H input.

The local oscillator produces the color subcarrier frequency 4.433619MHz (Fs) + 1/8 fH single frequency which goes to the sub converter. At the sub converter, the 40 fH and (Fs + 1/8 fH) are frequency converted to become (Fs + 40 fH + 1/8 fH). This is supplied through a highpass filter to the main converter. Also supplied to the main converter are the color signal Fs +0.6 −0.8 MHz and carrier wave (Fs + 40 fH + 1/8 fH). These are down converted to become (40 fH + 1/8 fH +0.8 −0.6 MHz) which through a lowpass filter goes to the mixer for mixing with the FM luminance signal. The result is applied to the video heads.

In other words, the 4.433619MHz (Fc) color subcarrier is converted to a low band of 626.953kHz (40 fH + 1/8 fH). The down converted color signal is then recorded directly using the FM luminance signal as AC bias.

(1) Color crosstalk correction by phase shift system

A synchronous quadrature modulation system is employed in which the phase of the color signal R-Y component is reversed every line in order to prevent transmission distortion.

The color signal indicated in Fig. 2-1-17 is converted to a lowband.

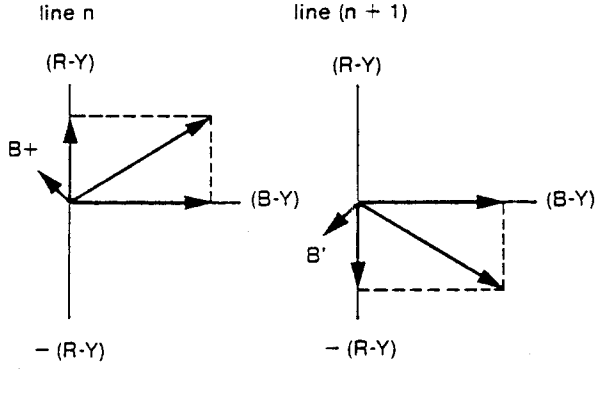


Fig. 2-1-17.

While the CH-1 track component is recorded with phase unchanged, the phase of the CH-2 track component is delayed 90° every line. Fig. 2-1-18 illustrates the principle of this phase shifts system.

In the figure, (a) indicates the phase shifted recording pattern. Since the CH-1 head pattern is not phase shifted, the R-Y component phase becomes inverted every line. The phase of the CH-2 head pattern is delayed every line and this causes its R-Y component phase to become inverted every two lines.

During playback, when the CH-1 head picks up a portion of the CH-2 track signal, this becomes the crosstalk component. Phase shift is not required for the main signal from the CH-1 track, and this output is shown by (b). The dotted arrows indicate the crosstalk component and, as can be noted, the phase reverses every 2 lines.

Passing signal (b) through a 2H delay line yields signal (c). In comparing signals (b) and (c), the main signal phase is the same every line, but the crosstalk phase reverses. Therefore, by mixing signals (b) and (c), the crosstalk component of the adjacent track can be removed to result in the playback color signal (d).

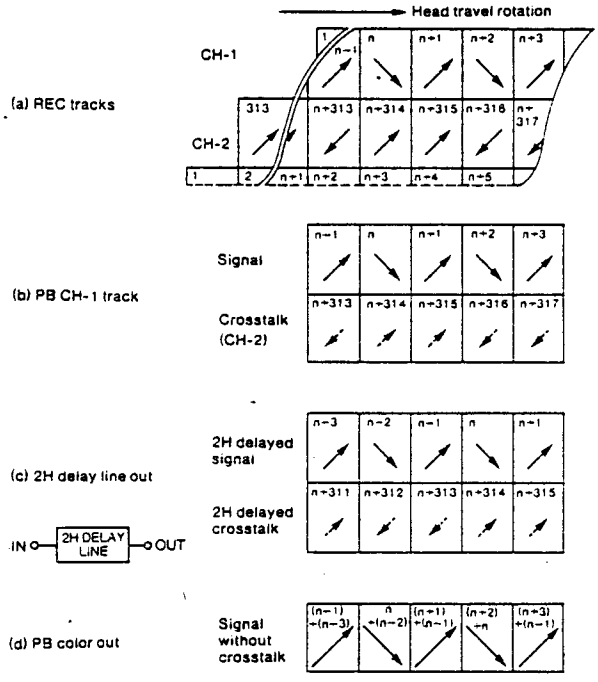


Fig. 2-1-18.

In other words, the color signal can be considered in 2H units. It is recorded by the phase shift system and during playback, the signal through a 2H delay line is mixed to remove crosstalk.
Crosstalk in the playback color signal (d) effectively becomes zero, while the main signal is enhanced to improve S/N. Also, the CH-2 head playback phase is advanced 90° every line (opposite to recording), producing the same effect. A digital type system is used for phase shifting.

(2) Down converted color subcarrier frequency
The color subcarrier frequency (Fs) can be expressed as:

$$Fs = (n-1/4)fH+1/625\ fH = 283.75\ fH + 25\ Hz$$

$$(n = 284) = 4.433619\ MHz$$

A line offset system is used in which the subcarrier phase is delayed 90° every line. This avoids serious color noise when the color signal is displayed on a monochrome TV receiver. 25Hz is added in order to prevent crosscolor.
As indicated in Fig. 2-1-18, the phase of the color signal R-Y component is inverted every horizontal line to compose a synchronous quadrature modulated signal. Fig. 2-1-19 shows this color signal spectrum.

In the phase shift system, the CH-1 component of the down converted color signal is distributed at 1/2 fH intervals centered on the Fc (down converted color subcarrier) component. The CH-2 track component is delayed in phase 90° every line, deviated by 1/4 fH, and distributed at 1/2 fH intervals centered on Fc. This spectrum is shown in Fig. 1-1-20.

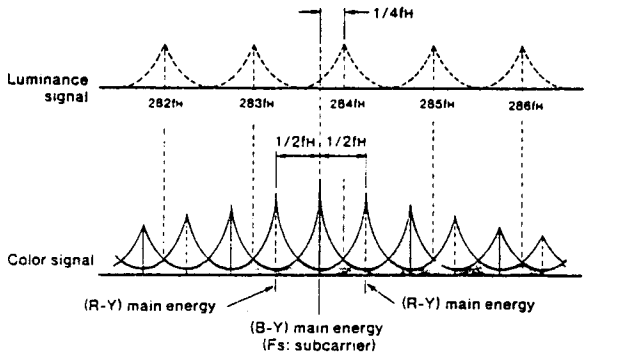


Fig. 2-1-19.

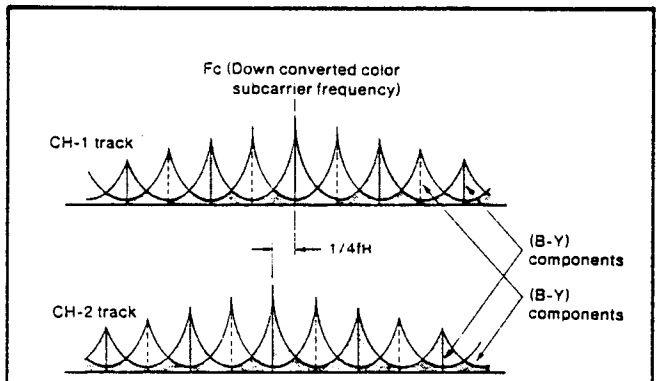


Fig. 2-1-20.

The FM luminance and down converted color signals are mixed to become the recording current. When recorded and played back using magnetic tape, which processes 3-dimensional distortion and nonlinearity, interference in the form of Fo + 2FDC (Fo: FM carrier; FDC: down converted color signal) becomes introduced and cannot be ignored. When the 2FDC component is detected and demodulated, beat becomes produced with respect to the luminance signal and appears in the picture. Therefore, as with the color signal, Fc (down converted color subcarrier frequency) must be selected so that the 2FDC component becomes 1/4 offset in relation to the luminance signal, i.e.:

$$2Fc = \frac{2n-1}{4} f_H$$

$$Fc = \frac{2n-1}{8} f_H = \frac{321}{8} f_H = 40\, f_H + \frac{1}{8} f_H \quad (n = 161)$$

$$= 625 + 1.953 = 626.953 \text{ kHz}$$

When Fc is determined at (40 fH + 1/8 fH), the spectrum of the CH-1 track B-Y component appears at (nfH + 1/8fH) and the R-Y component at (nfH − 3/8 fH). In the CH-2 track distribution, B-Y appears at (nfH − 1/8 fH) and R-Y at (nfH − 5/8 fH).

Fig. 2-1-21 shows the 2FDC component spectrum with respect to the playback luminance signal at this time.

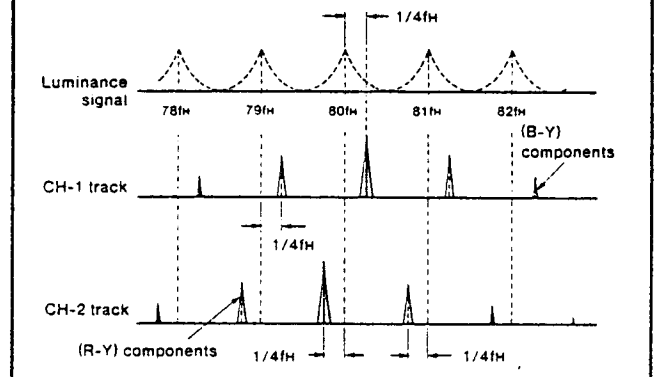


Fig. 2-1-21.

The 2FDC components for both CH-1 and CH-2 become 1/4 line offset with respect to the luminance signal and thereby visually reduced. The 626.953 value was selected for both reducing noise and in consideration of color bandwidth.

We have look at the principle of chrominance signal processing in some detail. The following sections describe the circuit functions according to signal flow. See Fig. 2-1-5 Chrominance Signal Block Diagram. The upper section in Fig. 2-1-5 shows chrominance signal path in recording mode and lower section shows playback mode.

2. 4.43MHz BAND-PASS FILTER (BPF) AND ACC CIRCUIT

The input video signal is applied to a differential circuit composed of C3026 and R3029 to remove the vertical sync component from it. The output of the differential circuit is input to a 4.43MHz BPF, where only the chrominance signal is extracted from the video signal. The output of the BPF goes to pin 4 of IC351.

The 4.43MHz chrominance signal is input an ACC amplifier and REC/PB switch, where the burst signal is extracted from it by burst gate pulse. The burst signal is applied to an ACC detector circuit, where a detection output corresponding to the burst signal level is taken out to control the ACC amplifier gain. As a result, the ACC amplifier output level variation is suppressed below ±0.5dB for an input level variation of ±6dB.

3. 4.433619MHz VOLTAGE CONTROLLED OSCILLATOR (VCO)

The 4.433619MHz oscillation is obtained by X351 crystal oscillation circuit. The oscillation frequency is adjustable with VR351 connected to pin 17 of IC351. The Rec APC circuit functions to lock the 4.433619MHz oscillation output phase with that of the burst signal from the ACC amplifier. This signal is also supplied to the killer detector.

4. 40fH SIGNAL GENERATION

After synchronization and separation by IC202 inside luminance P.C.B., the synchronization signal passes through the differential circuit of C3022, R3024 and R3025, and it becomes horizontal sync signal and equalizing pulse.

These signals are fed to IC351 pin 6, and is input to 1/2fH killer circuit where the equalizing pulse is removed. The remaining horizontal sync signal (fH) is input to rec AFC detector circuit which controls the phase of 160fH VCO.

To synchronize the 160fH VCO with the horizontal sync signal, the frequency of VCO is divided by 160 and its phase is compared with the horizontal sync signal. The resulting error voltage is used to phase correct the 160fH VCO. The circuit required is called AFC loop.
The 160fH pulse is divided by 1/4 divider to produce the 40fH pulse. The phase of 40fH pulse is delayed by 90° every 1H for CH2 while the phase for CH1 is unaltered.
The resulting 40fH signal is supplied to subconverter.

5. 4.435572MHz OSCILLATOR

The 4.435572MHz oscillator consists of a crystal element (X352) and an oscillator circuit (IC353).
The output of the oscillator is output from IC353 pin 9, and is input to the subconverter via pin 16 of IC351.

6. SUBCONVERTER

The 4.435572MHz and 40fH (625kHz) signals are applied to the subconverter, where they are mixed to produce a 5.06MHz and 3.81MHz signals, which are output from pin 18 of IC351. The signal then goes to a 5.06MHz BPF (L351), where only the 5.06MHz signal is extracted, and is input to pin 26 of IC351.

7. DOWN-CONVERTED CHROMINANCE SIGNAL

The 5.06MHz signal applied to pin 26 of IC351 is supplied to a main converter, where it is mixed with the 4.433619MHz chrominance signal from the ACC amp. The output of the main converter appears at pin 1 of the IC351.
The output signal at pin 1 contains two frequencies of 626.9kHz and 9.49MHz. This output is fed to a 1.5MHz LPF (L353), where a 626.9kHz down-converted chrominance signal is extracted. This signal is recorded on tape using the FM luminance signal as an AC bias.

2-1-6. CHROMINANCE SIGNAL PLAYBACK SYSTEM

1. GENERAL

The color signal playback system performs essentially the opposite function as the recording system. In addition, however, important corrections must be performed for color signal frequency and phase errors introduced by variations in tape speed and head rotation, and elasticity of the tape.
Fig. 2-1-22 indicates an abbreviated block diagram of this system.

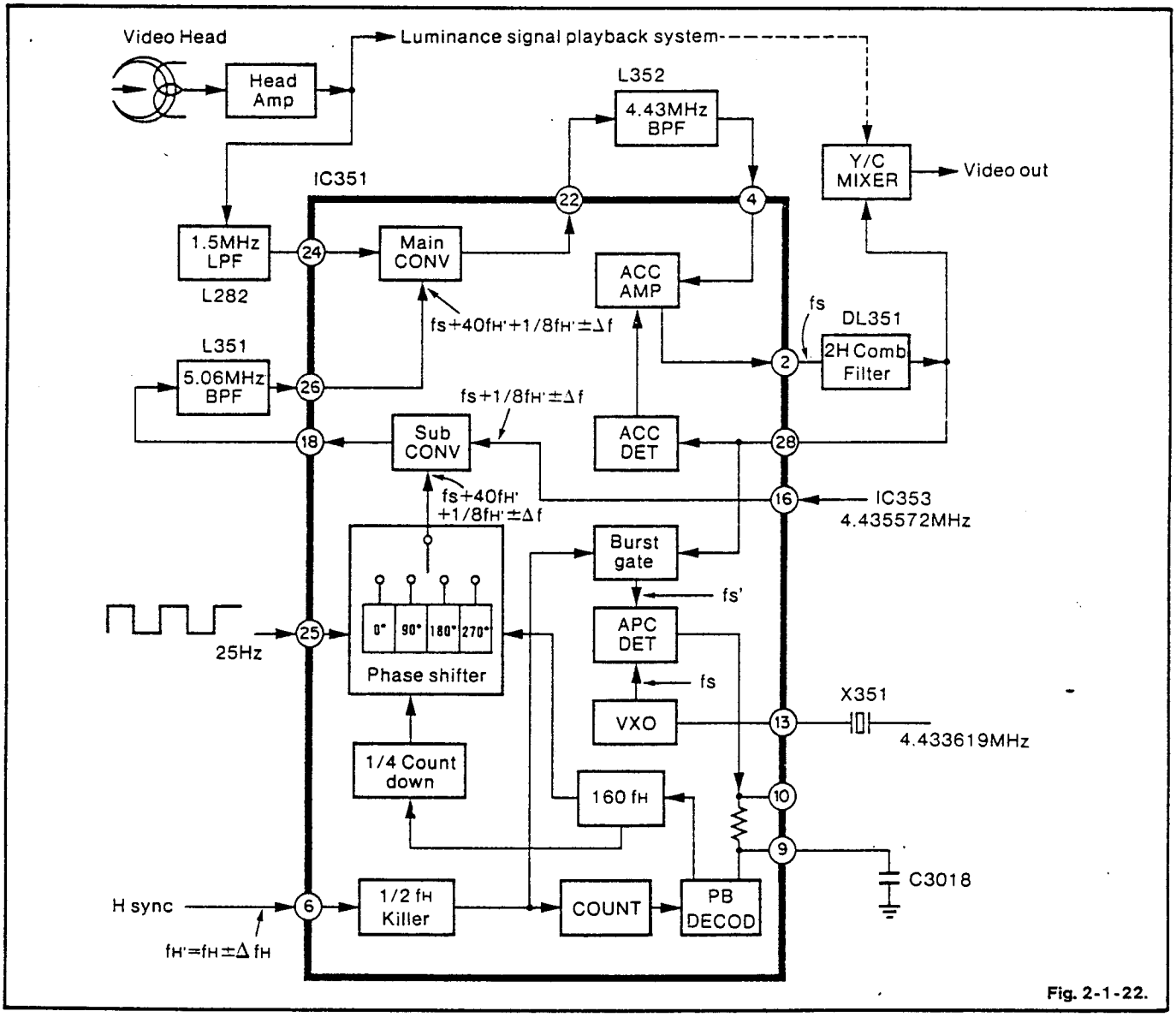


Fig. 2-1-22.

Though a lowpass filter, the down converted color signal goes to the main converter. At this time, the down converted color subcarrier (Fc) contains an error component (40 $f_{H'}$ + 1/8 $f_{H'} \pm \Delta f$) due to mechanical factors of the heads and tape. $f_{H'}$ varies with the tape speed as $f_{H'} \pm \Delta f_{H'}$. Δf is the instantaneous error caused by head rotation irregularities and tape elongation and contraction.
The 40 $f_{H'}$ frequency deviation component is compensated by supplying the video output signal to the horizontal sync separator, multiplier and phase shifter, and 40 $f_{H'}$ to the sub converter. This forms the AFC (automatic frequency compensator) loop.
In the APC (automatic phase compensator) loop, the 1/8 $f_{H'} \pm \Delta f$ phase error component is compensated by comparing the burst component of the up converted playback color signal with the subcarrier frequency from the local oscillator and APC detector. A variable crystal oscillator (VXO) produces (Fs + 1/8 $f_{H'} \pm \Delta f$) which goes to the sub converter. As a result, (Fs + 40 $f_{H'}$ + 1/8 $f_{H'} \pm \Delta f$) is supplied as the main converter carrier input from the sub converter through a highpass filter.
By frequency conversion with Fc, the color subcarrier frequency of 4.433619MHz, which is free from frequency and phase deviations, becomes obtained through a bandpass filter. In the opposite manner as with recording, the phase shifter advances the CH-2 track phase 90° every line and 40 $f_{H'}$ is supplied to the sub converter. The playback color signal through the main converter and bandpass filter is applied to a 2H delay line for removing crosstalk. Characteristics of the lowpass and bandpass filters are the same as those for recording.
At the mixer, the playback color and luminance signals are mixed to become the video output signal.

2. CHROMINANCE AND LUMINANCE SEPARATION

The down-converted chrominance signal is extracted from the envelope output of the video head by a 1.5MHz low-pass filter (L282) inside the luminance P.C.B. The output of the LPF is input to pin 24 of IC351 inside the chrominance P.C.B. via emitter follower (Q217, Q218, Q222).

3. 4.435572MHz SIGNAL GENERATION

Similar to the record mode, a 4.435572MHz signal is generated by a crystal-controlled oscillator, IC353 with X352. The signal is supplied from pin 16 of IC351 to the subconverter. The oscillating frequency is adjustable with a trimmer capacitor (C3103).

4. ID CIRCUIT

If phase switching point in playback chrominance signal does not match that in recording, a 180° of discontinuity will occur in the playback down-converted chrominance signal. This will cause a color flicker appearing in the upper section of the screen. The ID circuit is used to detect this discontinuity. The killer detector inside IC351 also functions as the ID detector.
The ID detector compares the 4.433619MHz VCO output with the burst signal contained in the playback chrominance signal. If a discontinuity occurs, the detector makes the same decision as in the monochrome mode, to generate a High level pulse at pin 23 of IC351.
This positive ID pulse is input to the emitter of Q363, and is output at its collector also as a positive pulse. The ID pulse then goes to pin 1 of IC351, drives a 40f_H inverter circuit to eliminate 180° of the discontinuity.

5. 40f_H GENERATOR

The synchronization signal is separated from the playback luminance signal by the sync separation circuit inside IC202, and is output from IC202 pin 3. This sync signal passes the differencial circuit (C3022 and R3025) and becomes horizontal sync signal. This signal is then supplied to IC351 pin 6.

The horizontal sync signal controls the phase of 160f_H VCO. The 160f_H is frequency divided by four, and the 40f_H is generated by the 4-phase rotator circuit.

6. SUBCONVERTER CIRCUIT

In the same way as at the time of recording, the 4.435572MHz from IC353 is supplied to pin 16 of IC351. This signal and 40f_H from the 4-phase rotator circuit are input to subconverter where they are mixed. The mixed output appears at pin 18 of IC351.

7. PB MAIN CONVERTER

The subconverter output apperating at pin 18 of IC351 goes through the 5.06MHz BPF (L351) where only the 5.06MHz frequency component is extracted.

This 5.06MHz is input to PB main converter via IC351 pin 26, while the down-converted playback chrominance signal (627 kHz) is also input to PB main converter via pin 24 of IC351.

Two signals are mixed with PB main converter and output from pin 22 of IC351.

8. ACC CIRCUIT

The PB main converter output appearing at pin 22 of IC351 is applied to a 4.43MHz BPF (L352), where its 4.43619MHz frequency component (chrominance signal of TV signal) is extracted. The output of the BPF is input to pin 4 of IC351 and enters the ACC amplifier. The output of the ACC amplifier appears at pin 2 of IC351, and goes to a 2H comb filter via an emitter follower (Q367). The 2H comb filter eliminates crosstalk from adjacent channels, and is input to the following amplifier (Q366).

For the details of the principle of crosstalk removal, refer to section 2-1-5.

The signal is sent to emitter follower (Q367) and then input to pin 28 of IC351, where it is coupled to an ACC detector circuit within the device. The ACC detector controls the ACC amplifier gain. Thus, an ACC loop is formed to regulate the chrominance signal level to a constant.

9. CHROMINANCE OUTPUT

The chrominance signal from the emitter follower (Q365) is input to IC202 pin 6 within the luminance circuit via PV362 pin 1 and PV213 pin 1.
The chrominance signal is mixed with the luminance signal in the mixer within IC202. The resulting TV signal is supplied to the RF converter and VIDEO OUT jack.

2-1-7. MESECAM OPERATION

The VTR is capable of recording and playing the SECAM B/G standard signals.
IC353 discriminates PAL/MESECAM signals. Figure 2-1-23 shows a block diagram illustrating the internal operations of IC353.

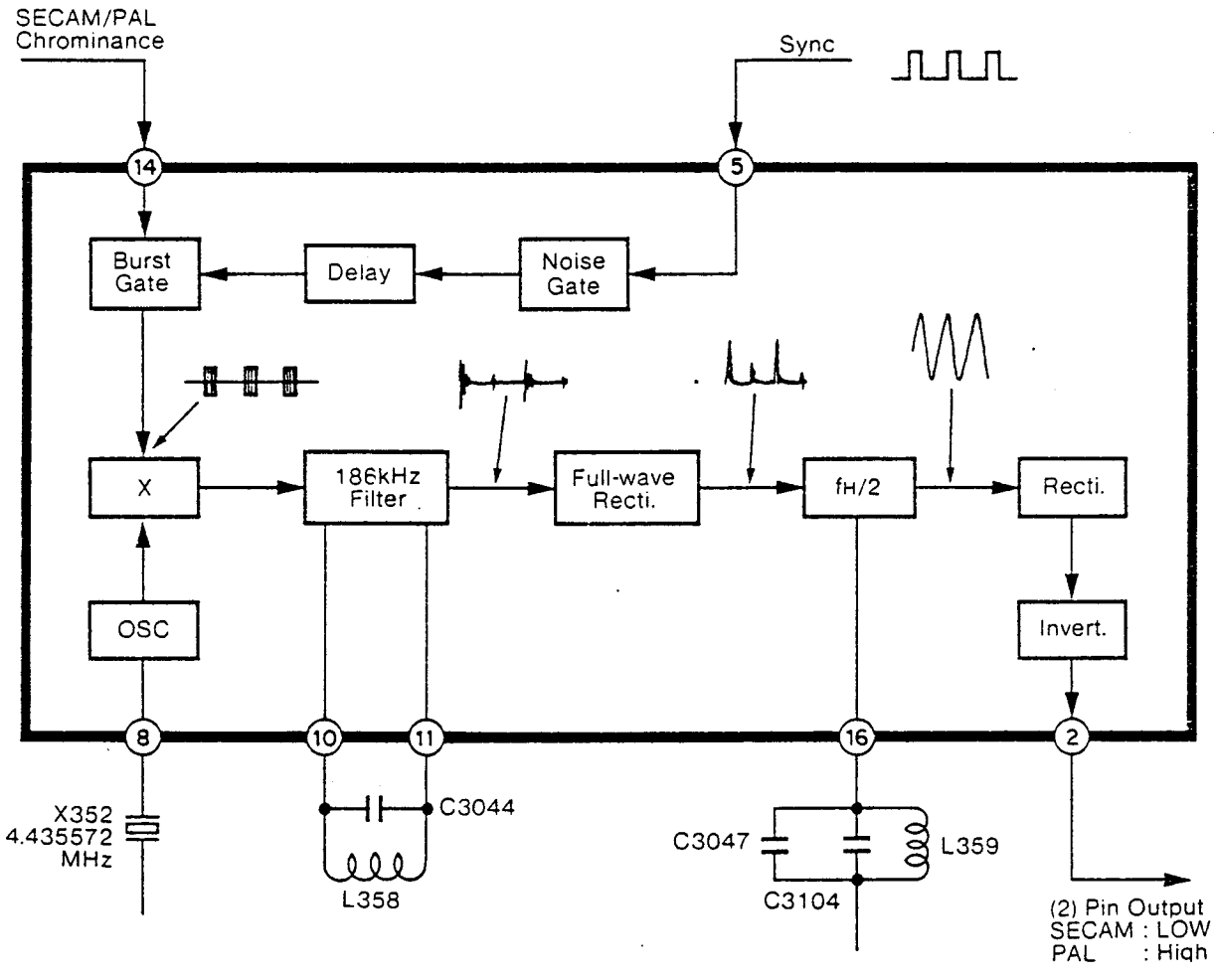


Fig. 2-1-23.

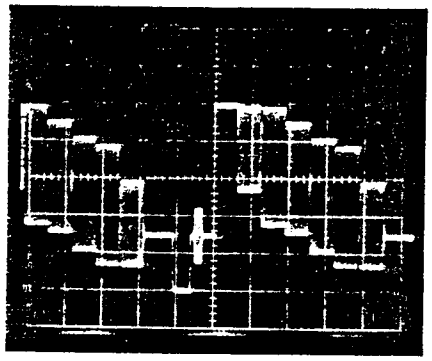
The color burst signal for the MESECAM signal has frequencies of 4.25MHz and 4.40625MHz, and is supplied at 1H intervals. The burst signal frequency is multiplied by the output frequency of a 4.435572MHz oscillator within the IC. If a 4.435572MHz filter (L358 and C3044) is used as a load, 4.435572MHz - 4.25MHz = 186kHz is obtained at the load. The output of the filter is subject to full-wave rectification to take out the fH/2 component (resonant circuit composed of L359, C3104 and C3047). The fH/2 component is rectified. The low output appears at pin 2 of IC353 via an inverter.

For the PAL signal, the 186kHz signal is not available as the 4.25MHz component does not exist. So pin 2 of IC353 remains at High.
The noise gate logic prevents the burst gate to be opened or closed at random due to sync signal disturned when the field strength is weak.

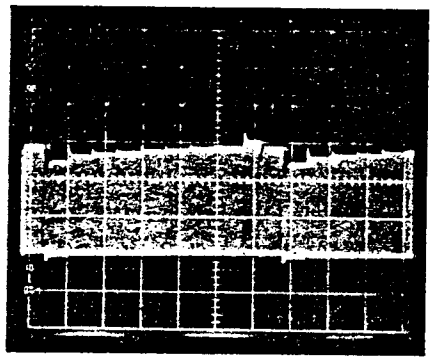
Since the MESECAM chrominance signal is an FM signal, it has no crosstalk from adjacent channels. It is not necessary, therefore, to shift the signal phase at 1H intervals, as is the case with the PAL signal. The 25Hz pulse is set to High by turning Q362 off. When pin 25 of IC351 is set to High, rotation of 40fH stops.
Playback of MESECAM signal requires no crosstalk removal using a 2H comb filter. Q369 is turned on to block the chrominance signal from the 2H comb filter.

2-1-8. VIDEO WAVEFORMS

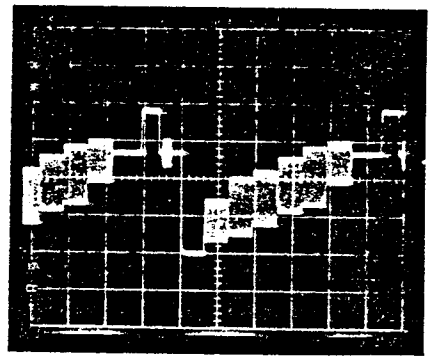
TP213 EE
200mV/10μsec div.



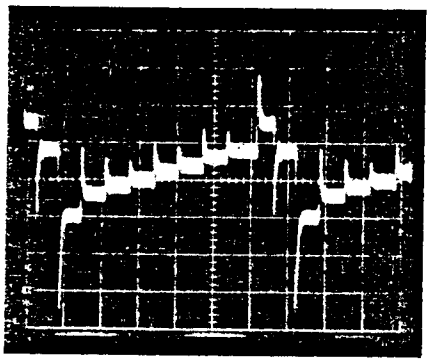
IC202 PIN 24 PB
1V/10μsec div.



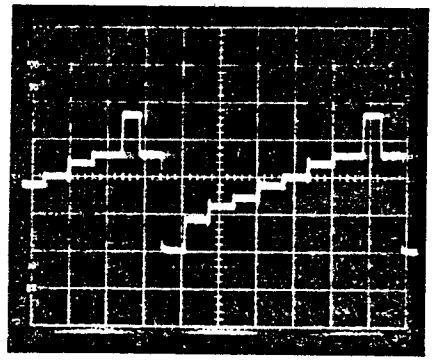
IC202 PIN 24 REC
200mV/10μsec div.



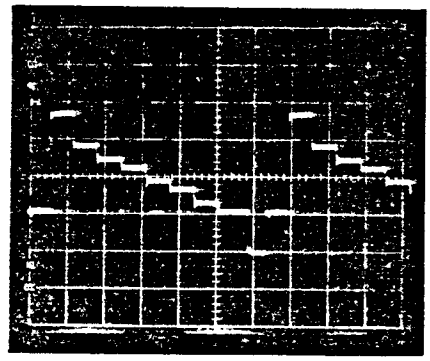
IC202 PIN 13 PB
100mV/10μsec div.



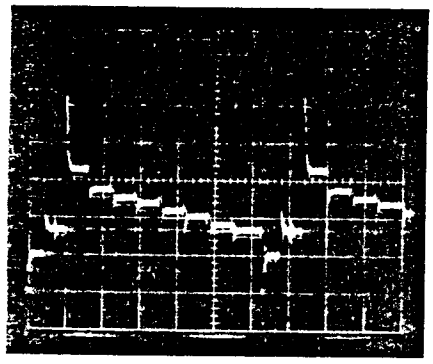
IC202 PIN 13 REC
100mV/10μsec div.



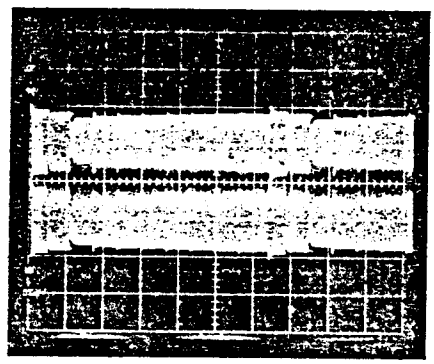
IC201 PIN 18 REC
200mV/10μsec div.



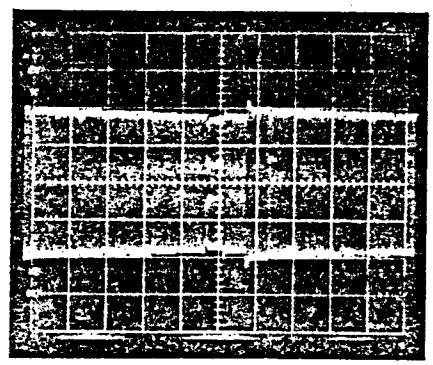
TP203 REC
200mV/10μsec div.



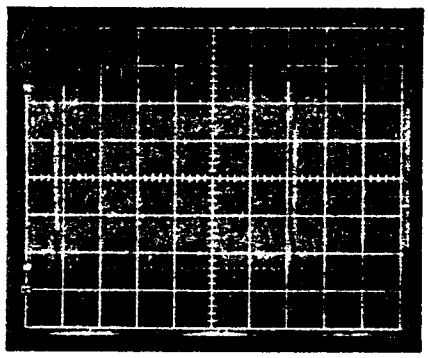
TP202 REC
200mV/10μsec div.



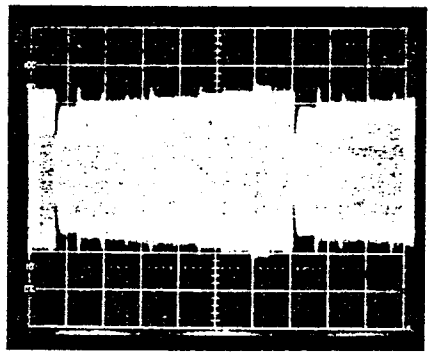
TP225 REC
1V/10μsec div.



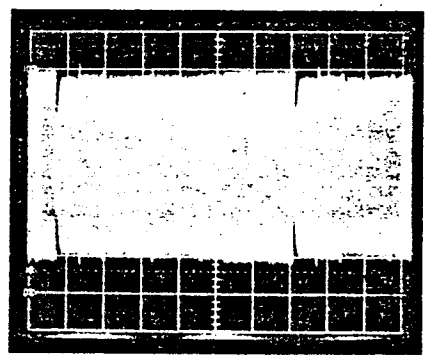
TP204 PB
10mV/10μsec div.



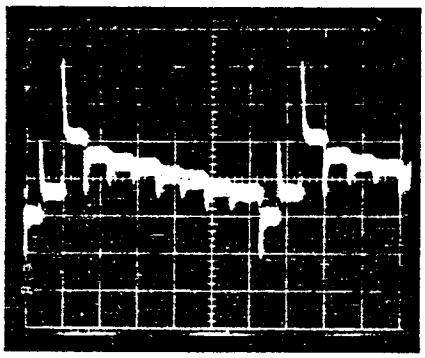
TP226 PB
50mV/10μsec div.



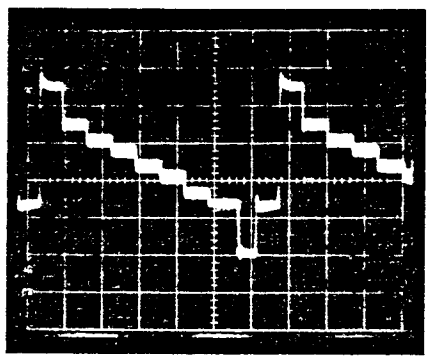
TP201 PB
100mV/10μsec div.



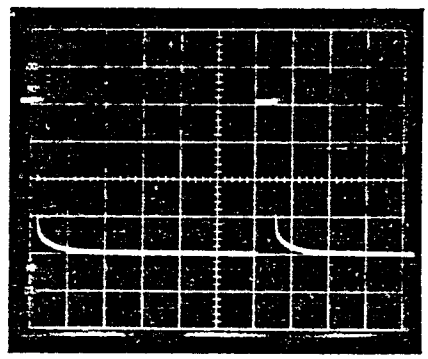
TP212 PB
50mV/10μsec div.



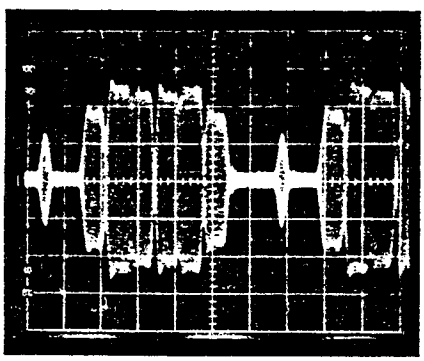
IC202 PIN 14 PB
200mV/10μsec div.



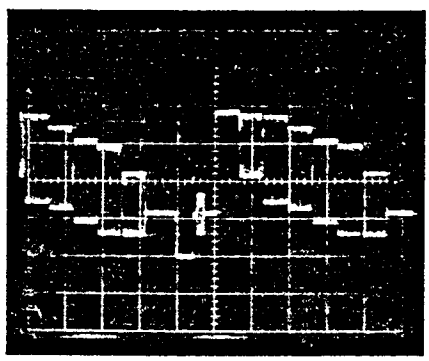
IC202 PIN 3 REC
2V/10μsec div.



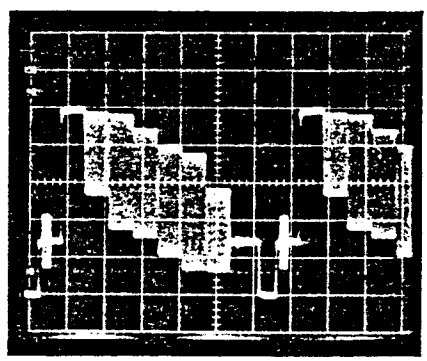
IC202 PIN 7 PB
50mV/10μsec div.



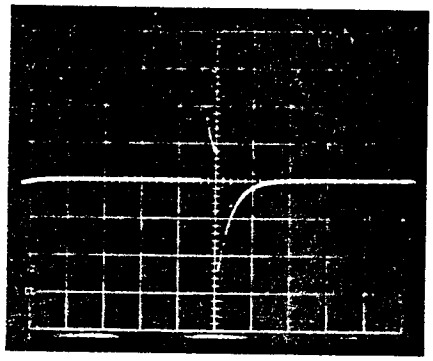
IC202 PIN 5 REC
500mV/10μsec div.



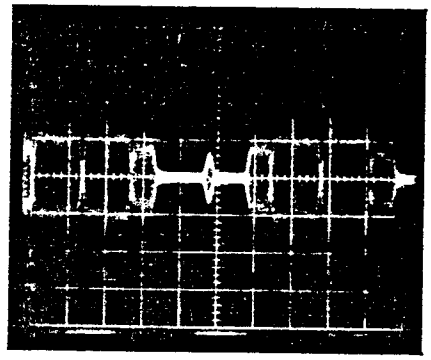
IC202 PIN 5 EE
200mV/10μsec div.



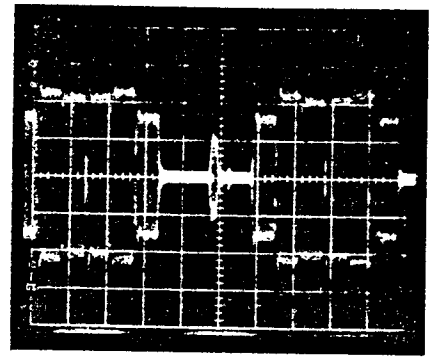
IC351 PIN 6 REC
1V/10μsec div.



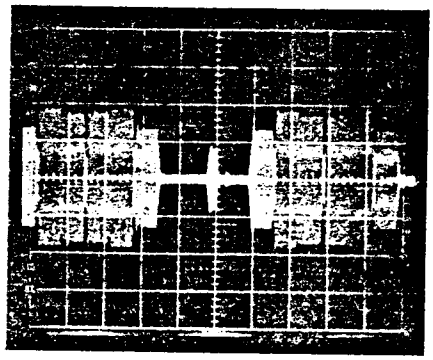
IC351 PIN 4 PB
100mV/10μsec div.



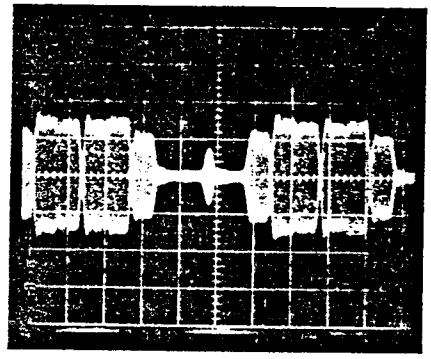
IC351 PIN 4 REC
50mV/10μsec div.



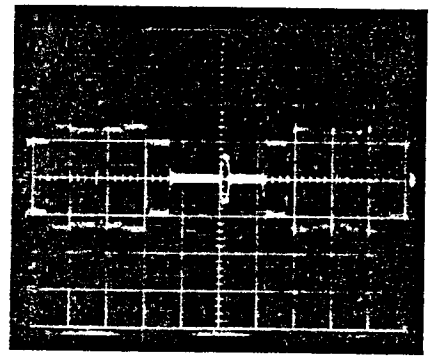
IC351 PIN 1 REC
200mV/10μsec div.



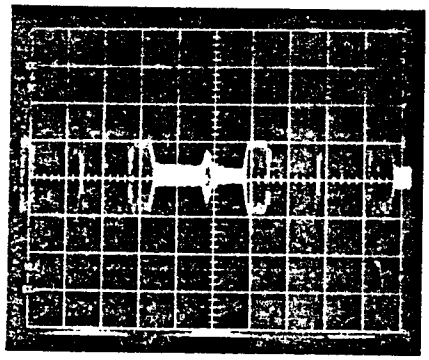
IC351 PIN 2 PB
500mV/10μsec div.



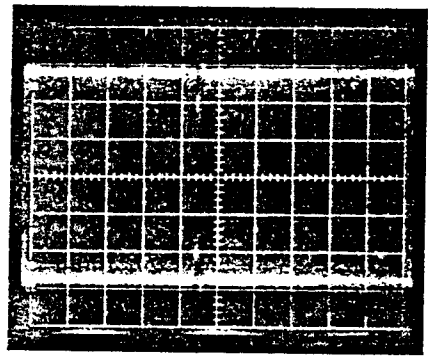
Q353 EMITTER REC
50mV/10μsec div.



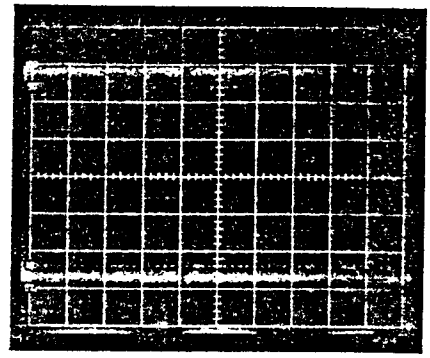
IC351 PIN 24 PB
100mV/10μsec div.



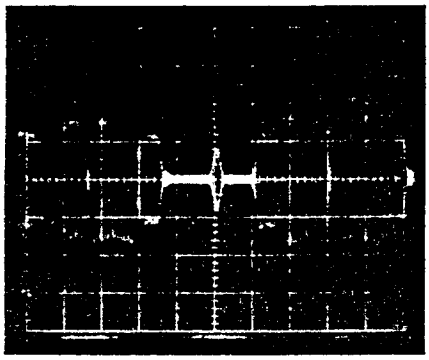
IC351 PIN 26 PB
50mV/10μsec div.



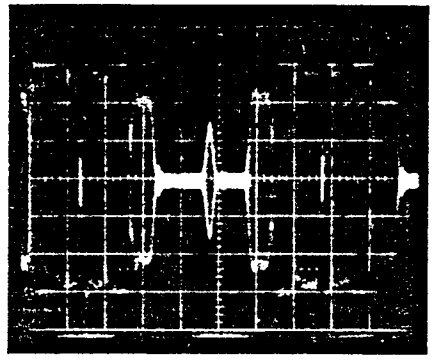
IC351 PIN 26 REC
50mV/10μsec div.



Q365 EMITTER PB
200mV/10μsec div.



PV362 PIN1 PB
200mV/10μsec div.



2-2. SYSTEM CONTROL CIRCUIT

2-2-1. GENERAL DESCRIPTION

1. FEATURES

1) The system control is a 2-clip configuration of the MAIN CPU and the SUB CPU of the N-ch MOS 42-pin. The SUB CPU is controlled by the transferred data from the MAIN CPU.

2) The operation of the mechanism is directly controlled by the MAIN CPU with the mode select switch and the front loading mechanism being controlled by the SUB CPU.

3) When the power is switched ON, the initialize operation controls the loading motor so that the mode select switch input is placed in the stop mode. If the tape is not loaded into the proper position in the front loading mechanism (stopped in the middle), the tape is ejected.

4) During unloading and ejecting, if the loading motor or the front loading motor is mechanically locked due to mechanical trouble, the motor power is automatically cut to prevent motor and drive IC damage.

5) During eject, tape slack is removed.

2. BLOCK DIAGRAM (See Fig. 2-2-1)

2-2-2. INPUT/OUTPUT SIGNALS DESCRIPTION

1. MAIN CPU INPUT SIGNALS

1) **A/D IN** — **Pin No. 2**
This input is determined by the function button being pressed (PB, REC, etc., excluding EJECT) as each button has a different resistance. The voltages generated by pressing the function buttons are A/D converted.

2) **MODE 1-3** — **Pins No. 30-32**
This input expresses the mechanism modes such as the STOP mode, PB mode etc., as well as controlling the operational timing of the mechanism during shifts from one mode to another.

3) **TAPE END DETECTION**
ESS — **Pin No. 22**
Supply reel side tape end detection.
Active with the high input.
EST — **Pin No. 23**
Take up reel side tape end detection.
Active with the high input.

4) **MECHANISM DETECTION SW**
CDT/SW — **Pin No. 37**
Detects the cassette when the cassette holder is in down position. Input is low when the SW becomes active.
SAFETY — **Pin No. 38**
If the safety tab has been removed, the input becomes low and does not allow REC.

5) **TROUBLE DETECTION**
DEW — **Pin No. 39**
Input becomes high when dew condensation is detected inside the set; the set is placed in the STOP mode. At the same time, the DEW LED blinks and does not allow key inputs. When the input becomes low, the blinking stops and key inputs are allowed.

6) **CAMERA CONTROL**
CP DIS — **Pin No. 4**
If input is high, the control input signals from the camera are not accepted.
CP ON/OFF — **Pin No. 5**
If input is high when the CP DIS input is low, the pause mode is established; if input is low, the pause mode is disengaged.

7) **TIMER INPUT**
TIMER REC — **Pin No. 34**
The set is placed in the REC mode if the REC conditions are met and the input is high. At this time, key inputs are not allowed.

8) **POWER CONTROL INPUT**
PWR ON — **Pin No. 33**
Input becomes low when the PWR ON SW is pressed; the PWR CONT output becomes low and power is supplied to all circuits.

9) **EJECT IN** — **Pin No. 35**
Input becomes low when the eject key is pressed; other key inputs are blocked.

2. MAIN CPU OUTPUT SIGNALS

1) **CAPSTAN MOTOR CONTROL**
CAP LO — **Pin No. 19**
Rotates the capstan motor at low speed to remove the tape slack.
CAP HI — **Pin No. 18**
Rotates the capstan motor at high speed during FF and REW.
REVERSE — **Pin No. 11**
Runs direction signal for the capstan motor. The motor runs in forward direction (clockwise) when this is high and in reverse direction (counterclockwise) when low.
SEARCH — **Pin No. 10**
Rotates the capstan and cylinder motors at high speed when this is low, and effective in cue or review operation.

2) **LOADING MOTOR CONTROL**
LOAD — **Pin No. 12**
When output is low, the loading motor is driven in the CCW (loading) direction.
UNLOAD — **Pin No. 13**
When output is low, the loading motor is driven in the CW (unloading) direction.
SLOW LOAD — **Pin No. 14**
When output is high, the motor speed is reduced to control the mode select switch operation precisely.

3) **COIL ON** — **Pin No. 15**
When output is high, the coil is energized and reel brake is held in released condition.

4) **ASR** — **Pin No. 3**
Outputs assemble record signal when changing from pause to record mode.

5) **TAPE COUNTER CONTROL**
T REVERSE — **Pin No. 16**
When output is low, it commands the tape counter to count down. (with R CUT correction)

6) **STOP MODE** **Pin No. 17**

Outputs a signal to recognize the SUB CPU that the mechanism is in STOP mode. When output is low, the mechanism is in the STOP mode.

7) **DATA TRANSFER**

CLK **Pin No. 25**
The clock signal when transferring data to the SUB CPU.
D0-D3 **Pins No. 26-29**
Data transfer bus to the SUB CPU.

8) **POWER CONTROL**

PWR CONT **Pin No. 24**
When the PWR IN input is low, a low is output to the power circuit, and +9.5V, +15V are supplied.

3. SUB CPU INPUT SIGNALS

1) **TROUBLE DETECTION**

CYL LOCK **Pin No. 6**
While the VCR is operating, the input pulse frequency is 30 Hz. When the STOP button is pressed, the input pulse frequency changes to 15 Hz and the VCR is automatically placed in the STOP mode. When the VCR stops, the input pulse frequency changes to 0 Hz. Check is started when loading is completed.
REEL LOCK **Pin No. 29**
Drive detection of the take up reel.
The set is placed in the stop mode if a drive signal is not received from the take up reel for 1.5 seconds during FF, REW, and 7 seconds during PB, REC. Check is started when loading is completed.

2) **MECHANISM DETECTION SW**

LSP SW **Pin No. 9**
Input is high when the cassette holder is in down position.
EED SW **Pin No. 10**
Input is high when the cassette holder is up; input becomes low when the tape is inserted.
CDT SW **Pin No. 2**
Input becomes low if the cassette holder is in down position and the cassette detection SW becomes active.

3) **EJECT SW** **Pin No. 11**

Input becomes high when the EJECT key is pressed.

4) **STOP MODE** **Pin No. 38**

Recives an input from the MAIN CPU. When the input is low, the mechanism is in the STOP mode.

5) **DATA TRANSFER**

CLK **Pin No. 37**
Clock signal for data transfer from the MAIN CPU.
D0-D3 **Pins No. 33-36**
Data transfer bus from the MAIN CPU.

4. SUB CPU OUTPUT SIGNALS

1) **LED INDICATORS**

PB LED **Pin No. 17**
During PB or REC mode, low is output and the PB LED lights up.
REC LED **Pin No. 16**
During REC mode, low is output and the REC LED lights up.
PAUSE LED **Pin No. 14**
During STILL, REC or PAUSE, low is output and the PAUSE LED lights up.
DEW LED **Pin No. 13**
When dew is detected, high and low are output alternately and the DEW LED blinks.
CST LED **Pin No. 18**
When the CDT SW input is low, low is output and the TAPE IN lights up.

2) **SERVO CIRCUIT CONTROL**

PB OUT **Pin No. 22**
Low output during PB.
REC OUT **Pin No. 23**
Low output during REC.
PAUSE OUT **Pin No. 24**
Low output during PAUSE.
LOAD OUT **Pin No. 25**
Low output during loading.
C DRIVE **Pin No. 4**
Low output during capstan motor rotation.
CYL ON **Pin No. 3**
Low output during cylinder motor rotation.
F ADV OUT **Pin No. 5**
High output during STILL.

3) **EJECT OUT** **Pin No. 39**

Output becomes low when the EJECT key is pressed and informs the main microcomputer that the mechanism should continue eject operations. Output returns to high after completing the eject sequence.

4) **KEY DIS** **Pin No. 19**

Holds the A/D IN input to low during front loading and eject, to prohibit key inputs.

5) **STOP PULSE** **Pin No. 32**

Makes a pulse output when the EJECT key is pressed, to place the set in the STOP mode.

6) **FRONT LOADING MOTOR CONTROL**

F LOAD **Pin No. 30**
When output is low, the front loading motor is driven in the CCW (front loading) direction.
EJECT **Pin No. 31**
When output is low, the front loading motor is driven in the CW (eject) direction.

7) **LSP** **Pin No. 8**

Outputs a low, high inverted LSP SW input signal.

8) **R CUT** **Pin No. 40**

This signal controls the T REVERSE, which commands the reel drive direction of the tape counter.

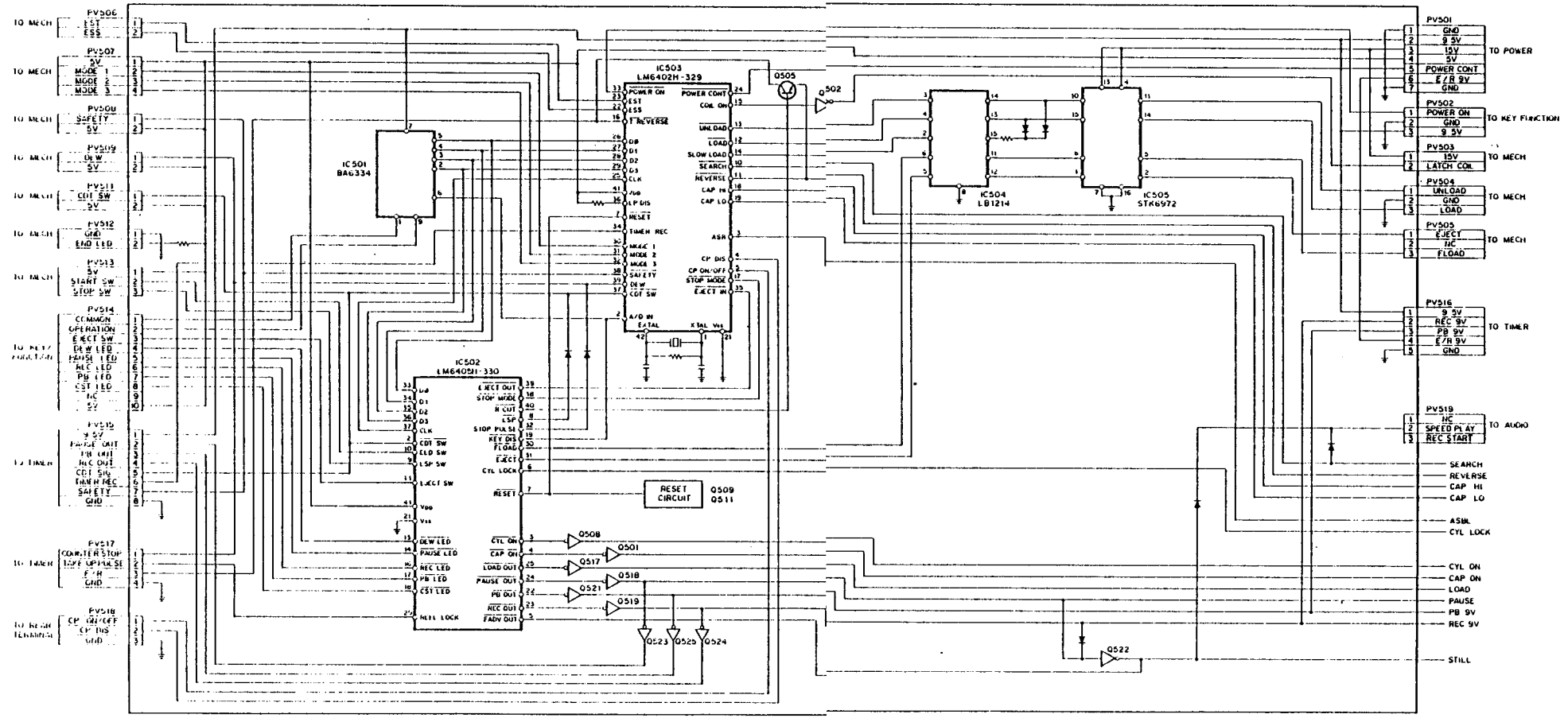

PV506
EST
ESS
PV507
5V
MODE 1
MODE 2
MODE 3
PV508
SAFETY
5V
PV509
DEW
5V
PV511
CDT SW
5V
PV512
GND
END LED
PV513
5V
START SW
STOP SW
PV514
COMMON
OPERATION
EJECT SW
DEW LED
PAUSE LED
REC LED
PB LED
CST LED
NC
5V
PV515
5V
PAUSE OUT
PB OUT
REC OUT
CDT SIG
REMOTE REC
SAFETY
GND
PV517
COUNTER STOP
LOAD UP PULSE
F/R
GND
PV518
CP ON/OFF
CP DIS
GND
TO MECH
TO KEY FUNCTION
TO TIMER
IC501
BA6334
IC502
LM6405H-330
IC503
LM6402H-329
IC504
LB1214
IC505
STK6972
Q501
Q502
Q505
Q508
Q509
Q511
Q517
Q518
Q519
Q521
Q522
Q523
Q524
Q525
RESET CIRCUIT
PV501
GND
9.5V
15V
5V
POWER CONT
E/F 9V
GND
TO POWER
PV502
POWER ON
GND
9.5V
PV503
15V
LATCH COIL
TO MECH
PV504
UNLOAD
GND
LOAD
PV505
EJECT
NC
FLOAD
PV516
9.5V
REC 9V
PB 9V
E/F 9V
GND
TO TIMER
PV519
NC
SPEED PLAY
REC START
TO AUDIO
SEARCH
REVERSE
CAP HI
CAP LO
ASBL
CYL LOCK
CYL ON
CAP ON
LOAD
PAUSE
PB 9V
REC 9V
STILL

Fig. 2-2-1

2-2-3. CIRCUIT DESCRIPTION

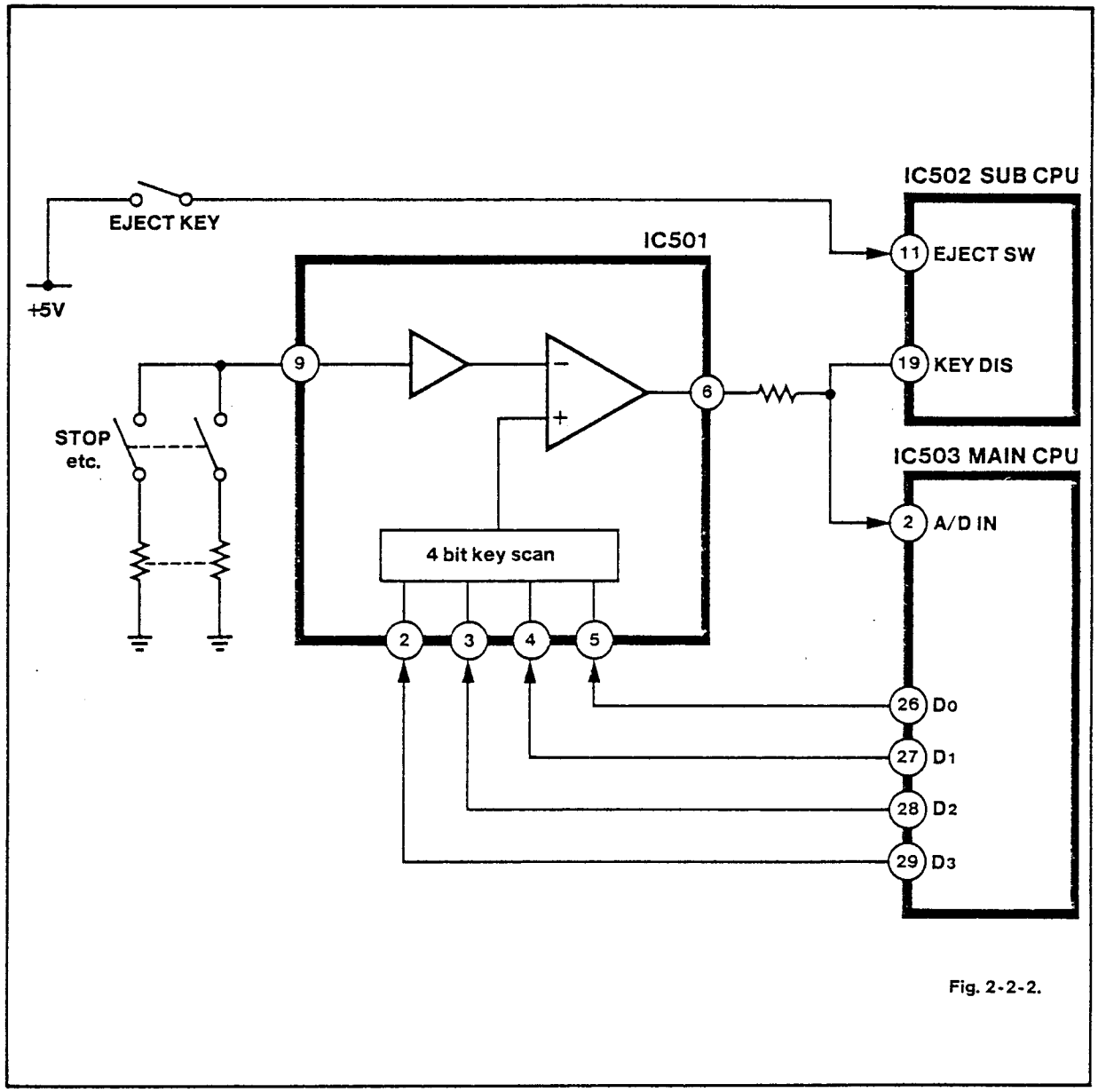


Fig. 2-2-2.

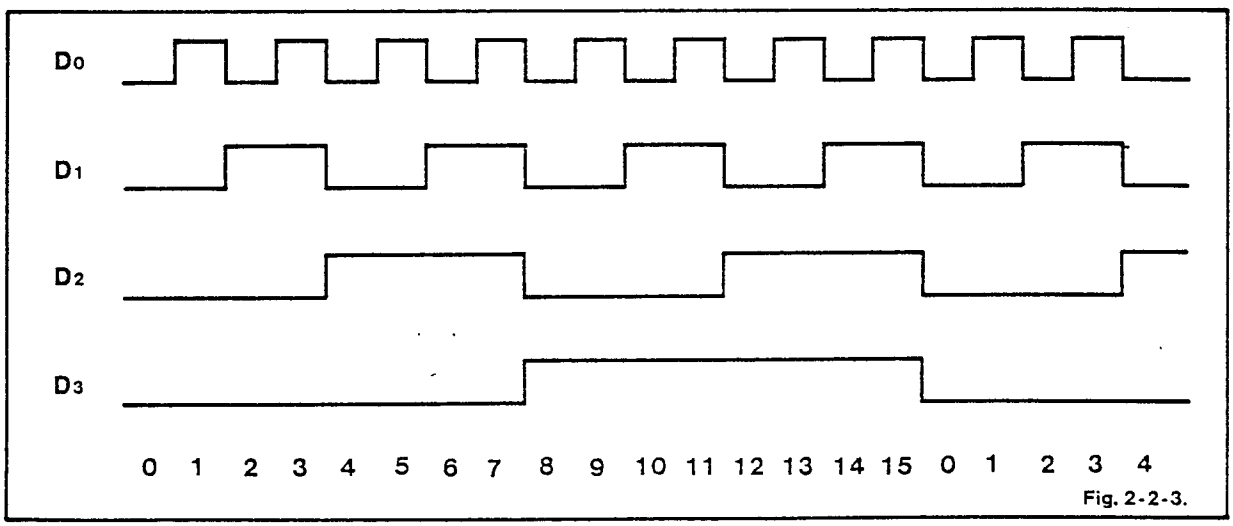


Fig. 2-2-3.

1. INPUT KEY DETERMINATION CIRCUIT (See Fig. 2-2-2 and 2-2-3)

When the OPERATION button is pressed on the front panel, IC502 pin 11 becomes high and the input is accepted. When buttons other than the OPERATION button are pressed, voltage corresponding to the respective button appears at IC501 pin 9, and the pin 6 output changes from low to high. When this output change is sent to the MAIN CPU IC503 pin 2, the outputs from IC503 pins 26-29 commence the count up operations, as shown in the timing chart. These are sent to IC501 pins 5-2, generating a step voltage at the non-inverted input of the built-in operational amplifier of IC501.

The voltage appearing at IC501 pin 9 is sent to the inverted input of the operational amplifier and is compared with the step voltage. This comparison is continued until the output from IC501 pin 6 changes from high to low.

When IC503 pin 2 input detects the change from high to low, the depressed button is identified according to the MAIN CPU program. The relationships between the D3-D0 count value and the input buttons are shown below. (See Table 2-2-1.)

CODE	D_3	D_2	D_1	D_0	OPERATION
0	0	0	0	0	
1	0	0	0	1	PB
2	0	0	1	0	REC
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	FF/CUE
10	1	0	1	0	REW/REV
11	1	0	1	1	STOP
12	1	1	0	0	SPEED
13	1	1	0	1	
14	1	1	1	0	PAUSE
15	1	1	1	1	

Table 2-2-1.

2. LOADING MOTOR, FRONT LOADING MOTOR DRIVE CIRCUIT (See Fig. 2-2-4)

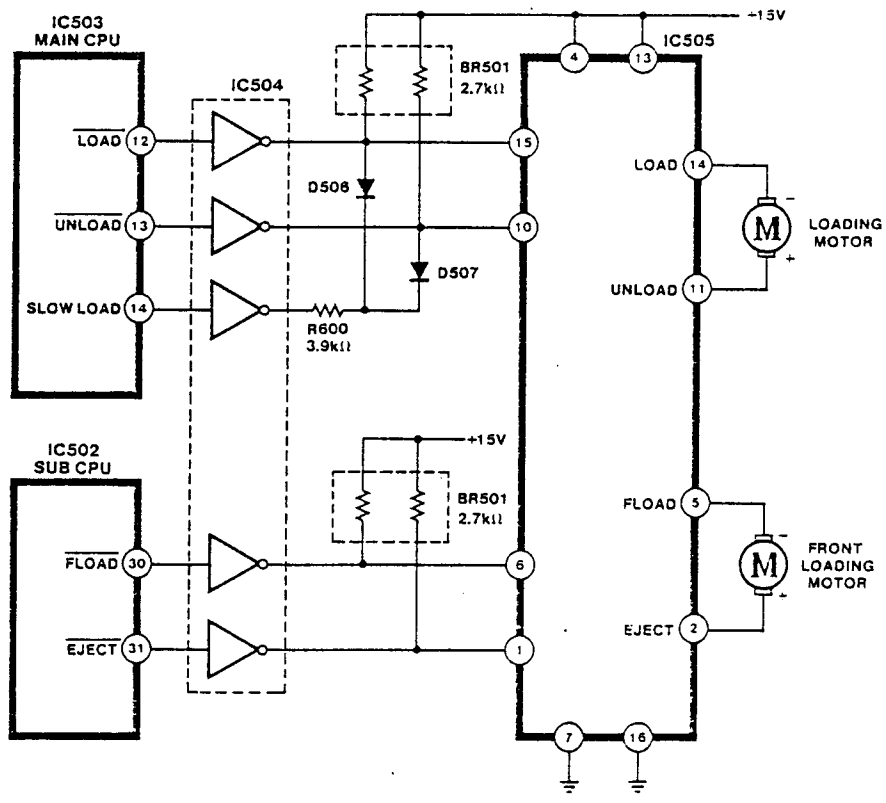


Fig. 2-2-4.

1) **LOADING**
When the IC503 pin 12 output is low and pin 13 output is high, the IC505 pin 14 output becomes approximately 13V and pin 11 output becomes 0V. The loading motor is driven in the CCW direction, placing the mechanism in the loading mode.

2) **UNLOADING**
When the IC503 pin 13 output is low and pin 12 output is high, the IC505 pin 11 output becomes approximately 13V and pin 14 output becomes 0V. The loading motor is driven in the CW direction, placing the mechanism in the unloading mode.

3) **SLOW LOAD**
When the IC503 pin 14 output becomes high, the terminal voltage of the loading motor is determined by comparing the various elements of BR502 and R600 and becomes approximately 8V for both loading and unloading. This is used to increase the detection precision of the mode select SW.

4) **FRONT LOADING**
When the IC502 pin 30 output is low and pin 31 output is high, the IC505 pin 5 output becomes approximately 13V and pin 2 output becomes 0V. The front loading motor is driven in the CCW direction, placing the mechanism in the front loading mode.

5) **EJECT**
When the IC502 pin 31 output is low and pin 30 output is high, the IC505 pin 2 output becomes approximately 13V and pin 5 output becomes 0V. The front loading motor is driven in the CW direction, placing the mechanism in the eject mode.

3. LATCH COIL DRIVE CIRCUIT
When the IC503 pin 15 becomes high, Q502 conducts, the latch coil is energized, and the reel brake is held in released condition.

4. TAPE COUNTER COUNT UP / DOWN COMMANDS (See Fig. 2-2-5)
The T REVERSE output makes a high or low signal output to the tape counter after being corrected by the logic between the REVERSE output and the R CUT output.
A high output is made to the tape counter during count up; a low output during count down.

Note: In the following descriptions, T REVERSE indicates the signal output made to the tape counter.

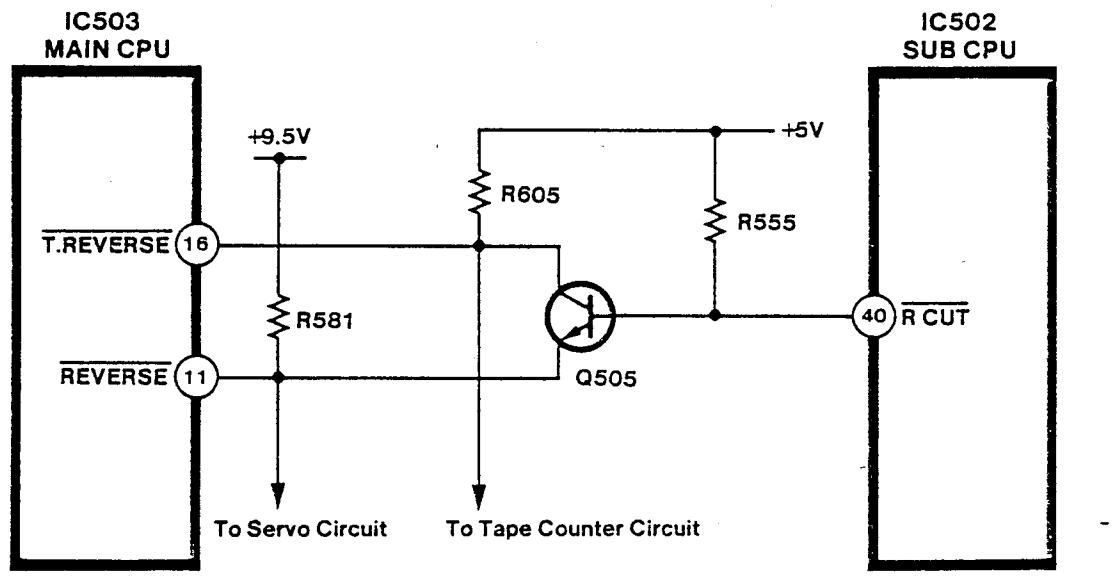


Fig. 2-2-5

2-2-4. OPERATION DESCRIPTION

1. MODE SELECT SW

The MODE SELECT SW is used as the mechanism position detection SW in the stationary mode and as the mechanism control signal input during the transition mode of the mechanism operation. (See Table 2-2-2)

Note: The arrow indicates detection at the edge. For 0 1, detection is made at the leading edge. (0: LOW LEVEL, 1: HIGH LEVEL)

	MODE 1	MODE 2	MODE 3
STOP MODE	0	1 → 0	0
REC PAUSE	1 → 0	1 → 0	0
REV	0	0	1 → 0
PB/REC/CUE	0 → 1	0	0 → 1

Table 2-2-2.

2. SOFTWARE TIMER

1) DURING LOADING

If the PB position is not detected within 5 seconds after commencing loading operations, the VCR automatically performs the unloading operations.

2) DURING UNLOADING

If the STOP position is not detected within 6 seconds after commencing the unloading operations, the loading motor is stopped.

3) If STILL, REC/PAUSE, or PAUSE are continued for more than 5 minutes, the VCR automatically starts to unload.

4) If REV is continued for more than 5 minutes, the set is placed automatically in the PB mode.

5) DURING FRONT LOADING

If the CDT SW low is not detected within 5 seconds after commencing front loading, the tape is automatically ejected.

6) DURING EJECT

If the EED SW high is not detected within 5 seconds after commencing eject, the front loading motor is stopped.

3. Table 2-2-3 Shows Sensor Operations

ESS	EST	OPERATION
H	H	Key input cannot be accepted.
L → H	L → H	STOP mode is entered immediately.
L	H	REW key input cannot be accepted.
L	L → H	STOP mode is entered immediately.
H	L	REW is entered by key input other than STOP and EJECT
L → H	L	AUTO REW is entered.
L	L	Normal operaion

Table 2-2-3.

4. TIMER RECORDING

	POWER IN	SAFETY	STAGE	ESS	EST
(1)	H	H	L	L	L
(2)	H	H	L	L	H

Table 2-2-4.

When the above conditions (1) or (2) are fulfilled, the set is placed in the REC mode when the TIMER REC input becomes high and the PWR OUT output becomes low.

When the TIMER REC input changes from high to low, the unload is stopped and the PWR OUT output becomes high. (See Table 2-2-4)

2-2-5. DESCRIPTION OF SPECIFIC OPERATIONS

1) INITIALIZE (See Fig. 2-2-6)

a) When the position data of the mode select switch are transmitted to the microcomputer, the loading motor runs in forward direction (CCW) for the following times: 100ms in PLAYBACK, 1s in EJECT (1, 0, 0) and 300ms in other modes. The latch coil is kept in the ON condition and the reel brake is released during this interval.

b) After 100ms, the capstan motor is driven slowly in reverse (CCW), shifting into the unload operations.
T REVERSE is set to low and tape counter starts count down.

c) When the MODE SELECT SW position [(0, 0, 0) - (0, 1, 0)] is detected, the latch coil and capstan motor are switched OFF. In addition, the slow load is output, making the loading motor unload slowly. At this time, brakes are applied to both reels.

d) When the MODE SELECT SW position [(0, 1, 0) - (0, 0, 0)] is detected, the reverse (CW) loading motor is stopped, the STOP MODE becomes low and the VCR is placed in the STOP mode.

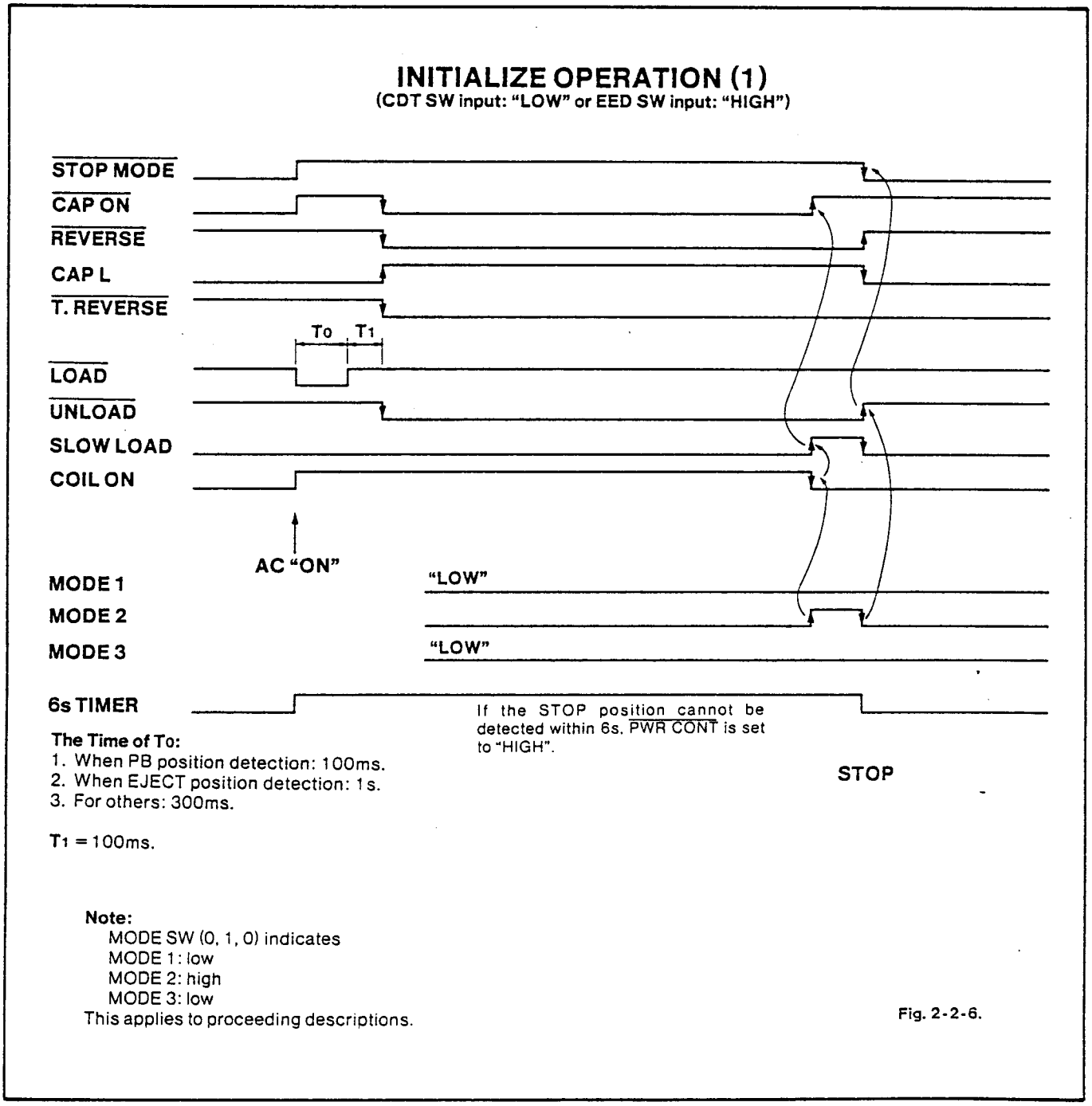


Fig. 2-2-6.

e) When the CDT SW input is low or the EED SW is high, the initialize operation is completed. (Fig. 2-2-7)

f) The EJECT OUT and KEY DIS outputs are made low. (See Fig. 2-2-7)

g) The LATCH COIL is switched ON, the loading motor loads for 100ms, the reel brake is disengaged and held in this condition. (See Fig. 2-2-7)

h) After 100ms, the capstan motor is driven slowly to take up tape slack. Count down command is sent to the tape counter. (See Fig. 2-2-7)

i) The front loading motor is driven in the CW direction and the eject operation is performed. (See Fig. 2-2-7)

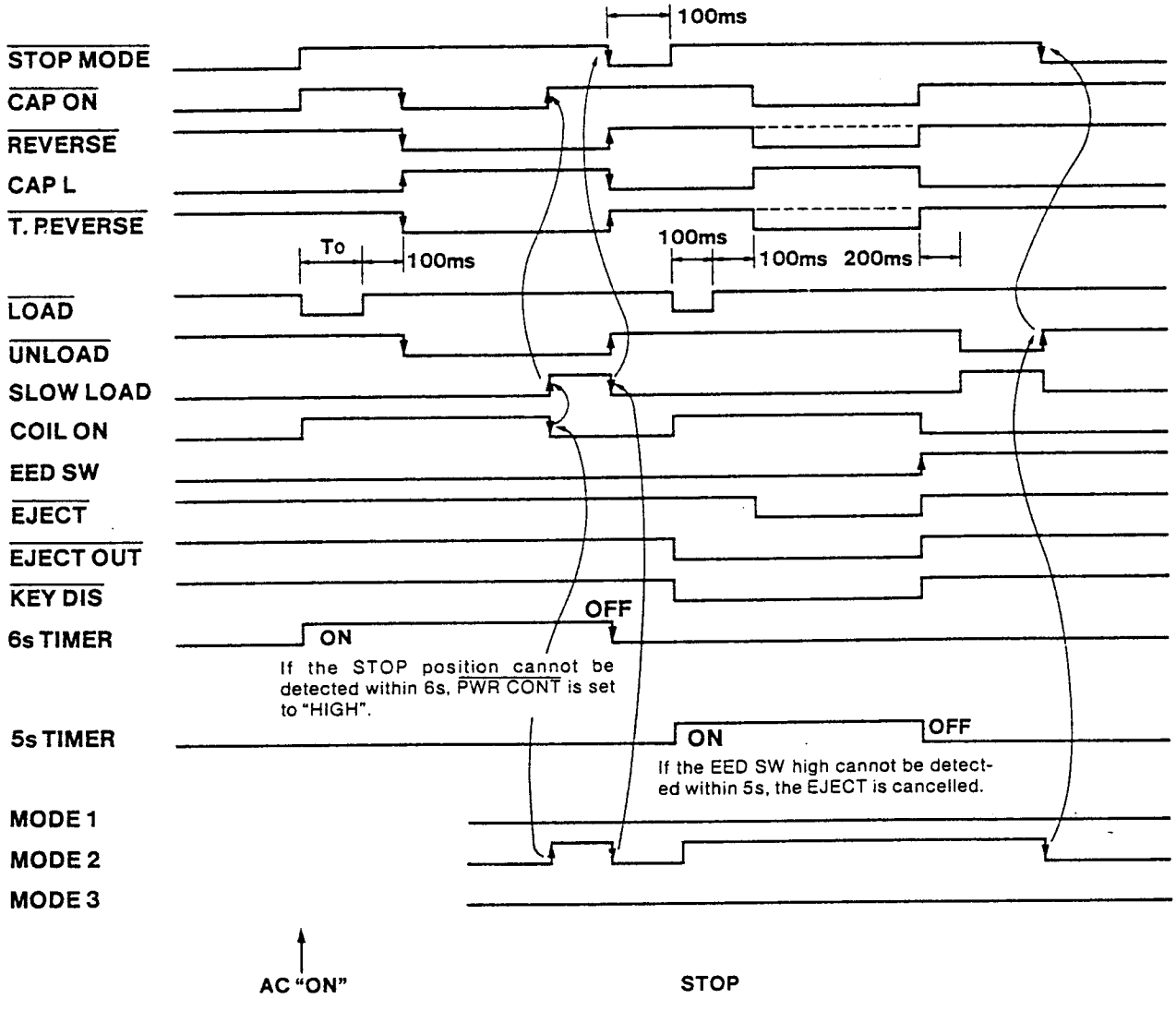
j) When the EED SW input high is detected, the LATCH COIL and capstan motor are switched OFF. In addition, the SLOW LOAD and EJECT OUT outputs become high, making the loading motor unload slowly. At this time, brakes are applied to both reels. (See Fig. 2-2-7)

k) When the MODE SELECT SW position [(0, 1, 0) - (0, 0, 0)] is detected, the loading motor drive is stopped, the STOP MODE signal is set to low and the set is placed in the STOP mode. (See Fig. 2-2-7)

INITIALIZE OPERATION (2)

(CDT SW input: "HIGH" or EED SW input: "LOW")

Dotted line indicates when "EST" is "HIGH".



The Time of To:

1. When PB position detection: 100ms.
2. When Mode Select Switch detects [1,0,0] position: 1s.
3. For others: 300ms.

Fig. 2-2-7.

2) LOADING (STOP — PB/REC) (See Fig. 2-2-8)

a) When the PB button alone or the PB and REC buttons are pressed simultaneously, the PB or PB and REC LEDs light up simultaneously.
At the same time:
1 CYL ON is set to low, starting the cylinder motor;
2 LOAD low, PB low or REC low outputs are sent to the servo circuit.
3 T REVERSE is set to low and output to the counter.
After 100ms, the loading motor is driven in the forward direction (CCW) and the loading operations are performed.

b) When the MODE SELECT SW position [(0, 0, 0) - (0, 1, 0)] is detected, T REVERSE is set to high and the capstan motor is driven in the forward direction (CW).

c) When the MODE SELECT SW position [(0, 0, 0) - (0, 1, 0)] is detected, the loading motor is stopped and the CYL LOCK, and REEL LOCK checks are commenced.

d) 1 second after c), the LOAD is set to high and the VCR is placed in the PB or REC stationary mode.

e) When the PB or PB and REC buttons are pressed simultaneously and the MODE SELECT SW position (1, 0, 1) is not detected, the VCR is placed in the unload mode.

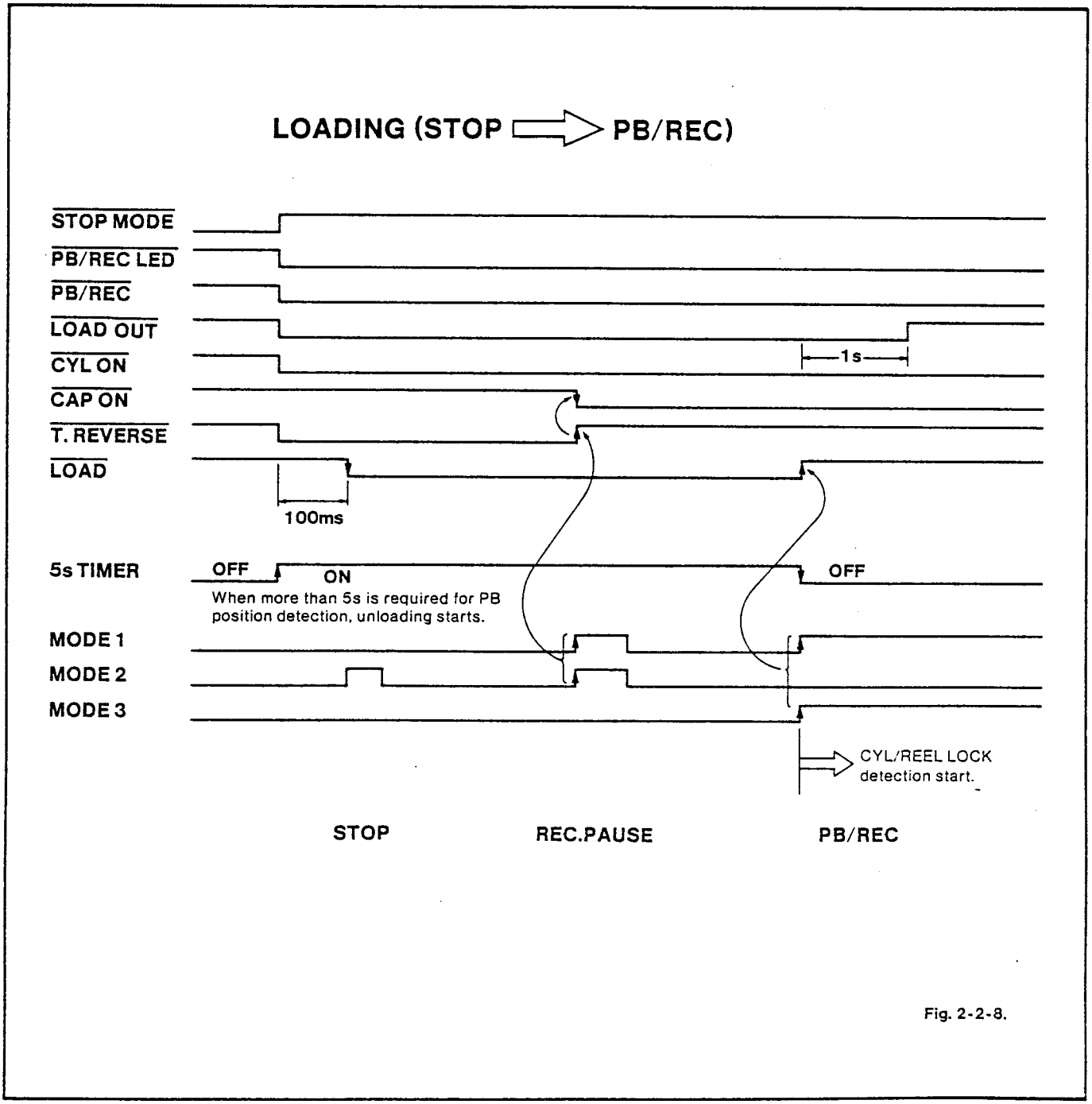


Fig. 2-2-8.

3) UNLOADING (PB/REC — STOP) (See Fig. 2-2-9)

When the STOP button is pressed during the PB (PB, CUE, REV, STILL) REC, or REC PAUSE mode the set is placed in the unload stop mode.

a) PB or PB and REC LEDs go out.
At the same time, PB or REC is set to high, as well as CYL ON, and the cylinder motor is stopped.

b) The LATCH COIL is turned ON, loading (CCW) is performed for 100ms, the brake is disengaged and maintained in this condition.

c) After 100ms, the loading motor is driven in the reverse direction (CW) and the unload operation is started.

d) When the MODE SELECT SW position [(0, 0, 0) - (1, 1, 0)] is detected, after a 200ms stop, the capstan motor is slowly driven in the reverse direction (CCW) to take up tape slack. T REVERSE is set to low.

e) When the MODE SELECT SW position [(0, 0, 0) - (0, 1, 0)] is detected, the capstan motor and the LATCH COIL are switched OFF and the loading motor is slowed down.

f) When the MODE SELECT SW position [(0, 1, 0) - (0, 0, 0)] is detected, the loading motor is stopped and the VCR is placed in the stop mode.

g) When the STOP button is pressed and the set is placed in the unload operation, the 6-second timer operates immediately. If the MODE SELECT SW position (0, 1, 0) is not detected within 6 seconds, the loading motor is stopped.
In this condition all button inputs and function SW inputs are not accepted.
The set is initialized by turning AC power on.

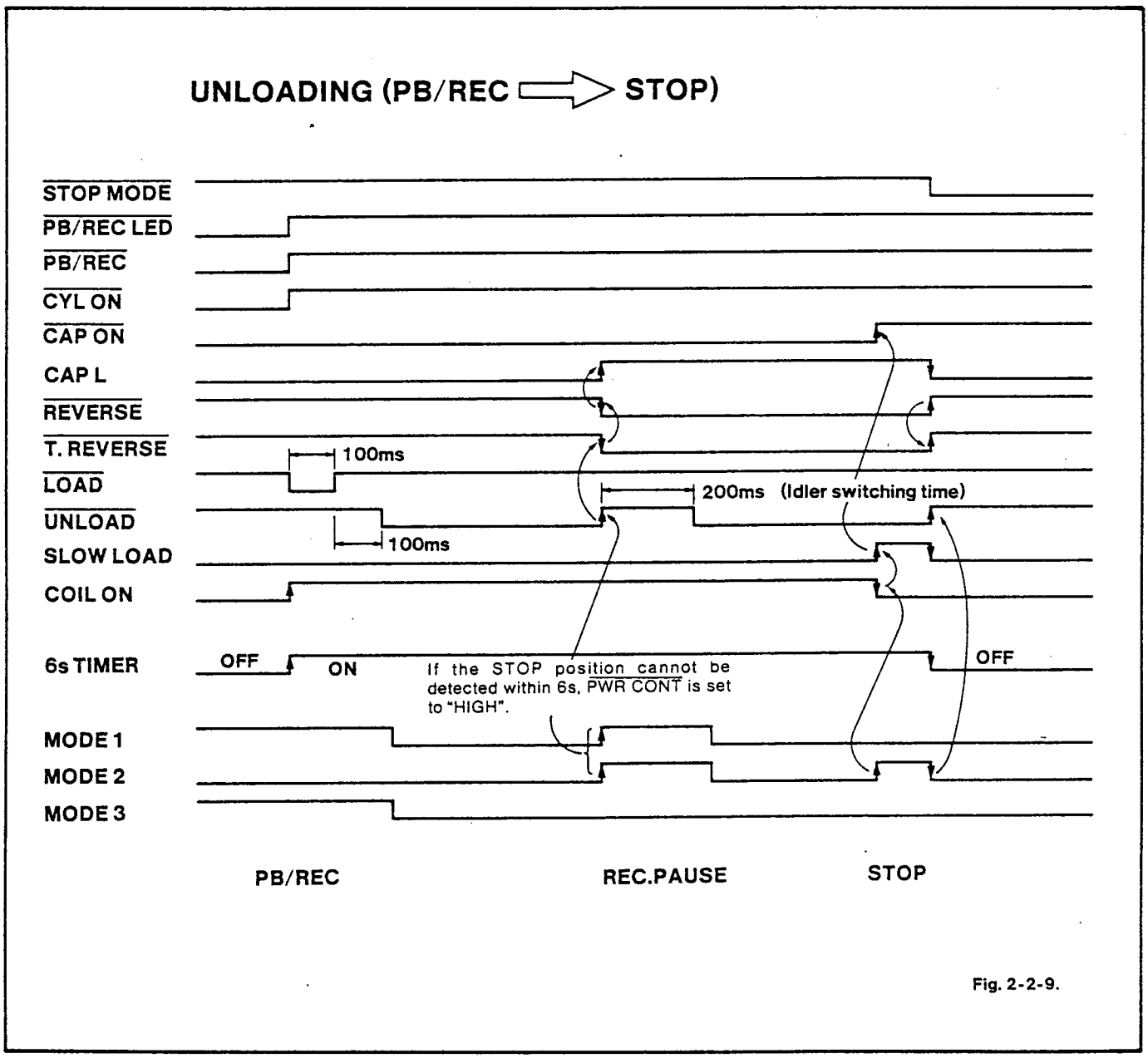


Fig. 2-2-9.

4) PB → STILL (See Fig. 2-2-10)

When the PAUSE button is pressed in the PLAYBACK mode, the capstan motor is stopped and the VCR is placed in the STILL mode.

a) PAUSE low is output to the servo circuit, and the PAUSE LED lights up at the same time.

b) A pulse of 98ms high and 2ms low is output for 1.5s to CAP ON for intermittent drive of the capstan motor.

c) If the STILL mode is continued for more than 5 minutes, the set automatically unloads, and stops.

5) STILL → PB (See Fig. 2-2-10)

a) When the PAUSE button is pressed in the STILL mode, PAUSE is set to high and the PAUSE LED goes out.

b) At the same time, F ADV, CAP ON are set to low and the capstan motor is driven in the forward direction (CW).

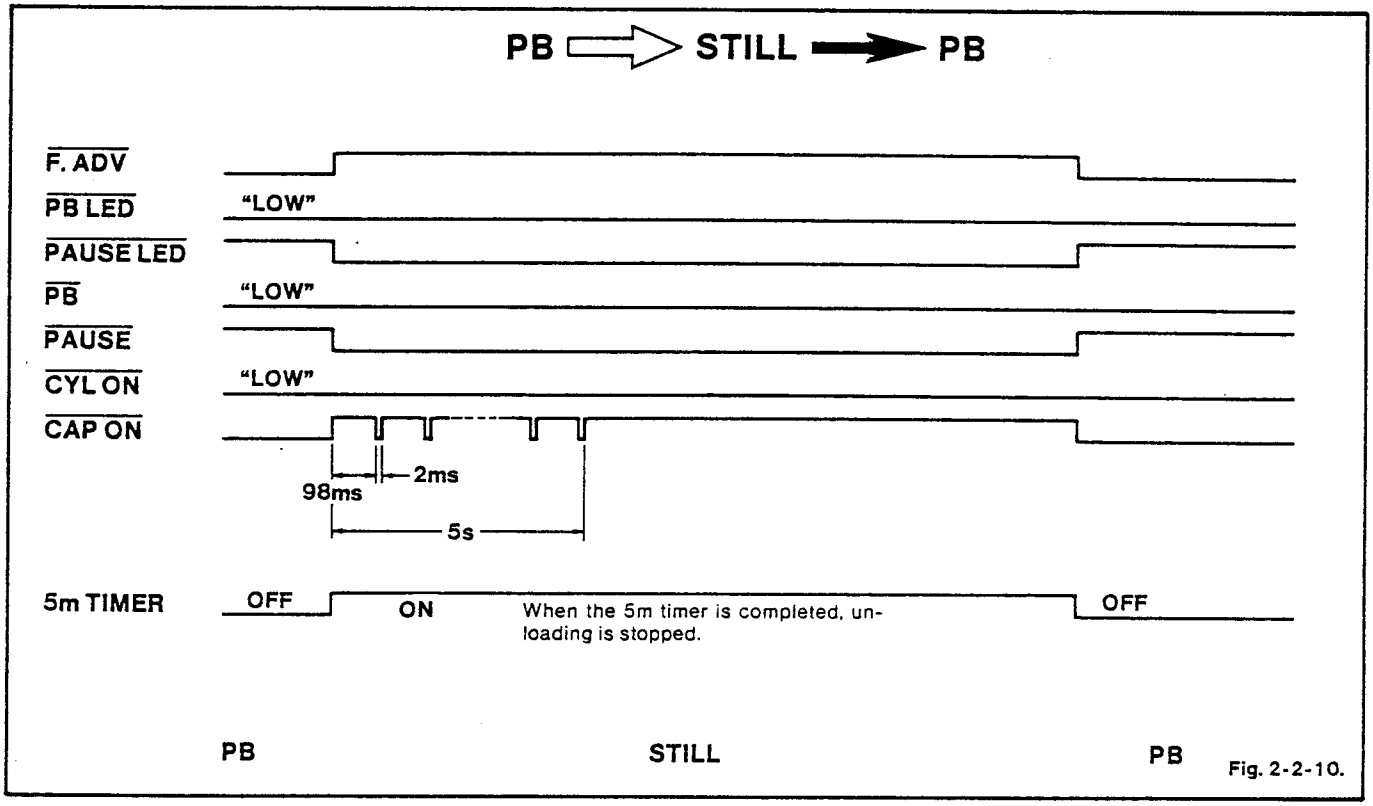


Fig. 2-2-10.

6) PB → CUE (See Fig. 2-2-11)

When the FF button is pressed in the PLAYBACK mode, SEARCH is set to low; the cylinder and the capstan motors run at high speed.

7) CUE → PB (See Fig. 2-2-11)

When the PB button is pressed in the CUE mode, SEARCH is set to high, and the VCR shifts to the PB mode.

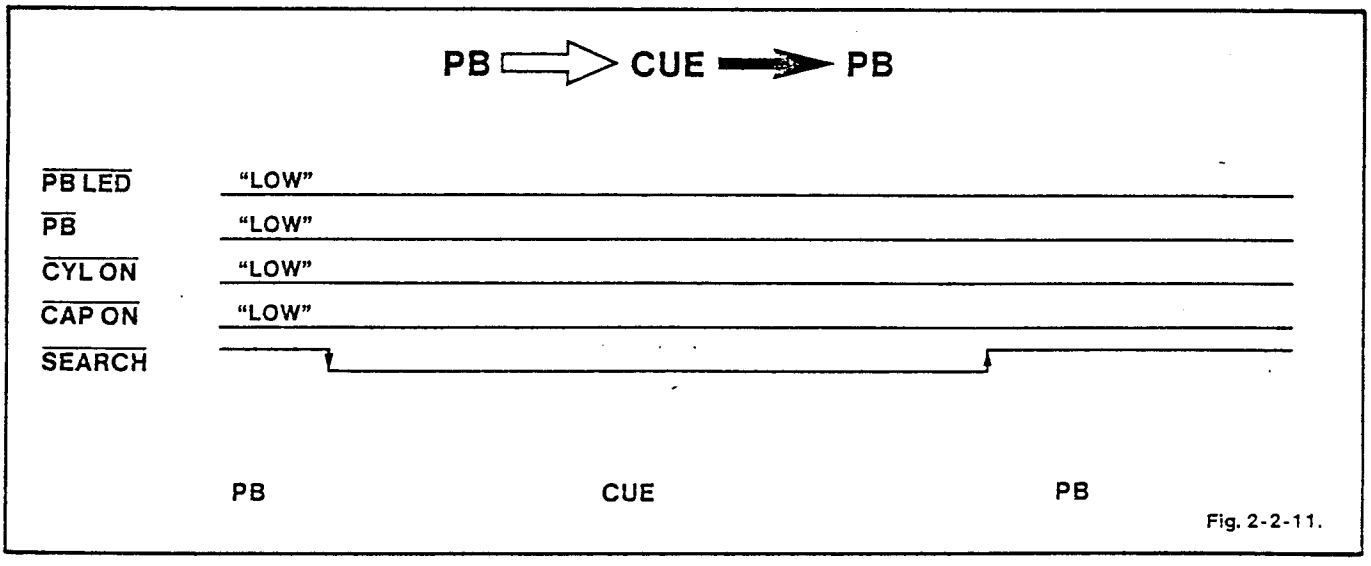


Fig. 2-2-11.

8) PB/CUE/STILL → REV (See Fig. 2-2-12)

When the REW button is pressed in either the PB CUE, or STILL modes the VCR is placed in the high-speed reverse playback mode after the following steps:

a) SEARCH is set to low and the capstan is driven quickly in the forward direction (CW). During this interval, STILL and CAP ON are set to low simultaneously, to maintain tape tension.

b) The loading motor is driven in the reverse direction (CW) and the pinch roller is separated from the capstan.

c) When the MODE SELECT SW position (1, 1, 0) is detected, the capstan motor is driven in the reverse direction (CCW) at normal speed and switches the idler to the supply reel side. The loading motor forward drive (CW) is stopped. T REVERSE is set to low and the counter starts count down.

d) After 100ms, the loading motor is driven in the forward direction (CCW) at low speed.

e) When the MODE SELECT SW position [(0, 0, 1) - (0, 0, 0)] is detected, the loading motor is stopped, SEARCH is set to low, the capstan motor is driven quickly in the reverse direction (CCW), the cylinder motor is driven at high speed; the VCR is placed in the REV stationary mode.

f) When the REV mode is kept continuously for more than 5 minutes, the VCR automatically reverts to the PB mode.

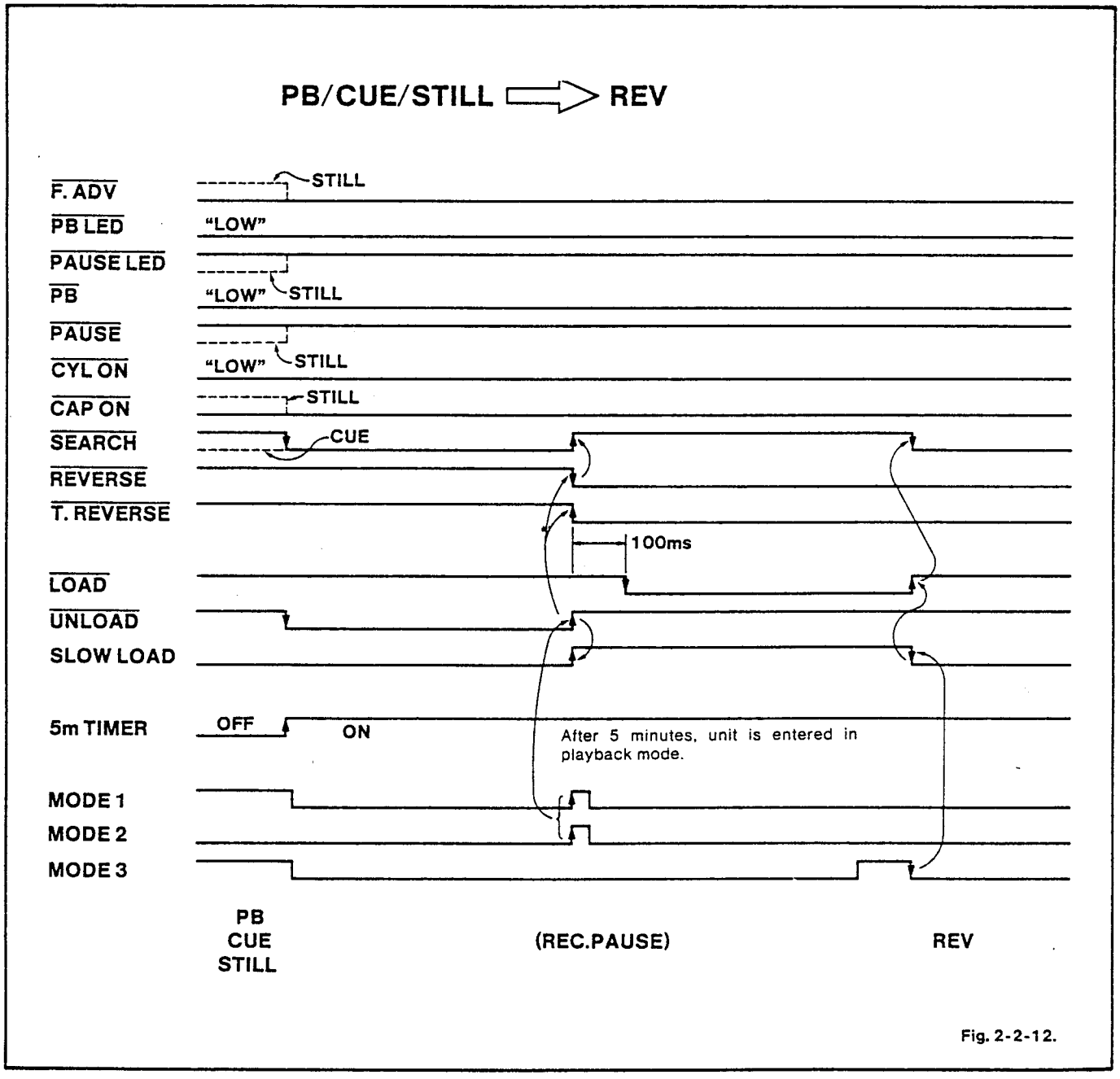


Fig. 2-2-12.

9) REV — PB/CUE (See Fig. 2-2-13)

When the PB button is pressed in the REV mode, the set shifts to the PB mode.

a) Until the MODE SELECT SW position (1, 1, 0) is detected, the loading motor is driven in the CW (unload) direction.

b) When the MODE SELECT SW position is detected, the capstan motor is driven in the forward direction (CW) and the idler is switched to the take up reel side. T REVERSE is set to high and the counter starts count up.

c) After 100ms, the capstan speed is driven at the normal speed (when shifting into CUE, SEARCH is kept low) and low speed loading (CCW) is performed.

d) When the MODE SELECT SW position (1, 0, 1) is detected, the loading motor is stopped and the VCR shifts into the PB or CUE stationary mode.

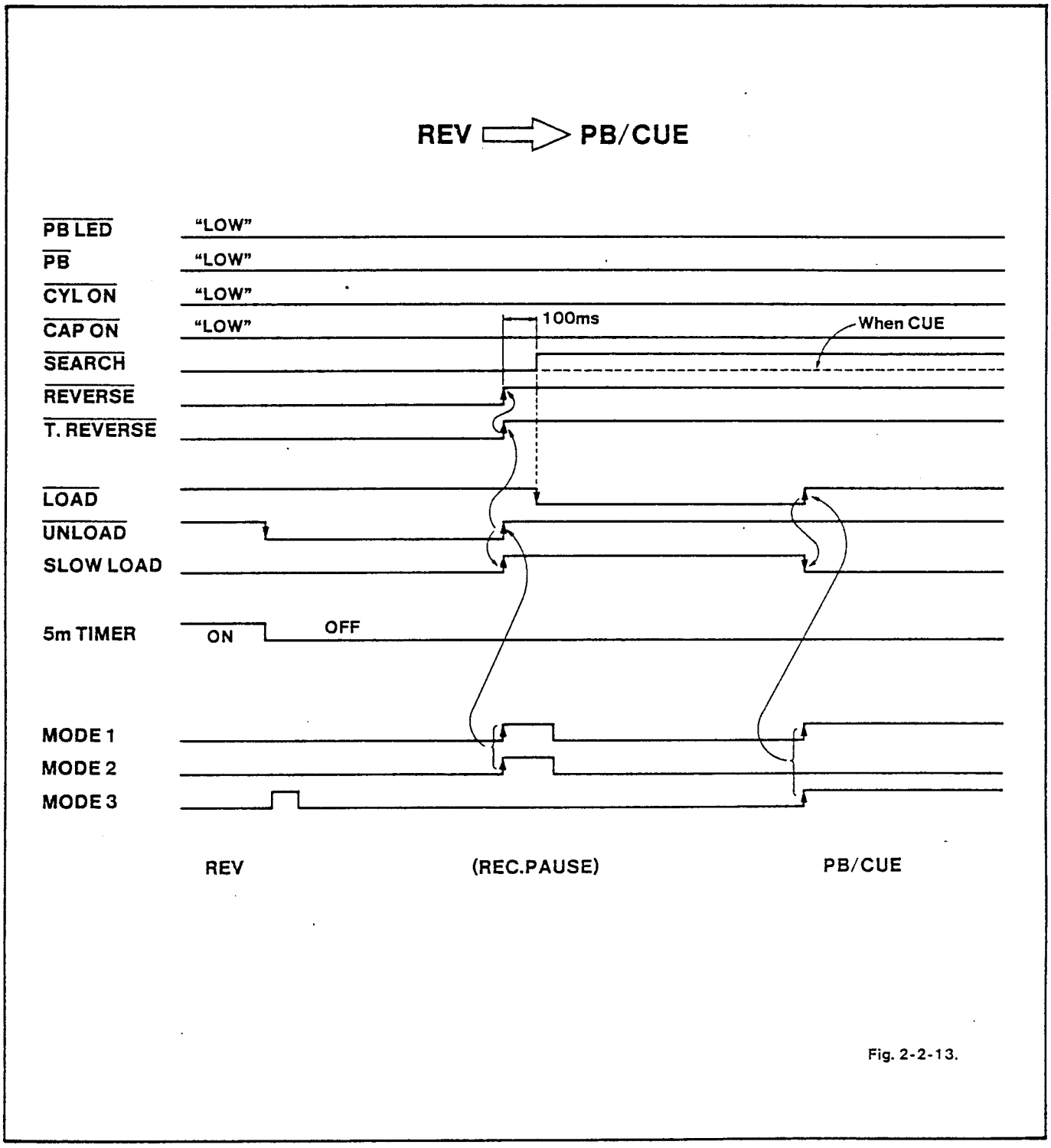


Fig. 2-2-13.

10) STILL → CUE (See Fig. 2-2-14)
When the FF button is pressed in the STILL mode, the VCR shifts into the CUE mode.

a) PAUSE high is output to the servo circuit.

b) SEARCH and CAP ON are set to low and the capstan motor is driven in the forward direction (CCW) quickly.

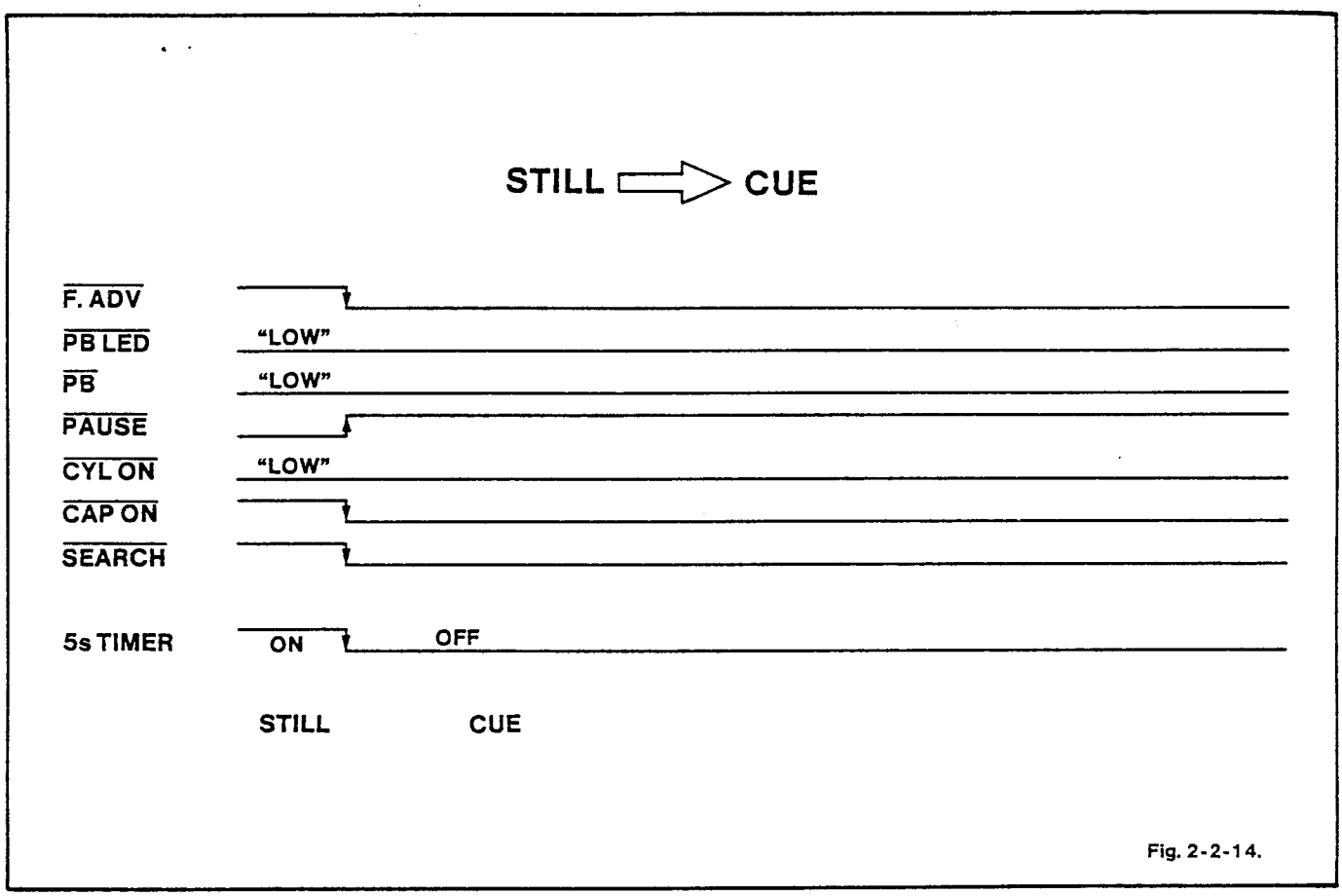


Fig. 2-2-14.

11) STILL/REC → REC PAUSE (See Fig. 2-2-15)

When the PAUSE button is pressed in the REC mode, the set shifts into the REC PAUSE mode.

a) The PAUSE LED lights up and PAUSE is set to low. (When shifting from STILL, F. ADV is low.)

b) The loading motor unloads (CW) until the MODE SELECT SW position (1, 1, 0) is detected.

c) The capstan motor is driven in the reverse direction (CCW) and the idler is switched to the supply reel side. T REVERSE is set to low.

d) After 100ms, the loading motor is driven in the forward direction (CCW) and the load operation is performed.

e) When the MODE SELECT SW position (0, 0, 1) is detected, the loading motor is stopped. At this time, it is in the REV position.

f) The tape is rewound in the reverse direction by the pinch roller for 1.5 seconds.

g) After 1.5 seconds, the loading motor unloads slowly (CW) until the MODE SELECT SW position (1, 1, 0) is detected.

h) Running of the capstan motor in the reverse direction (CCW) is stopped. T REVERSE is set to high.

i) After 100ms, the loading motor loads slowly (CCW) until the MODE SELECT SW position [(1, 1, 0) - (0, 0, 0)] is detected, and the VCR is placed in the REC PAUSE stationary mode.

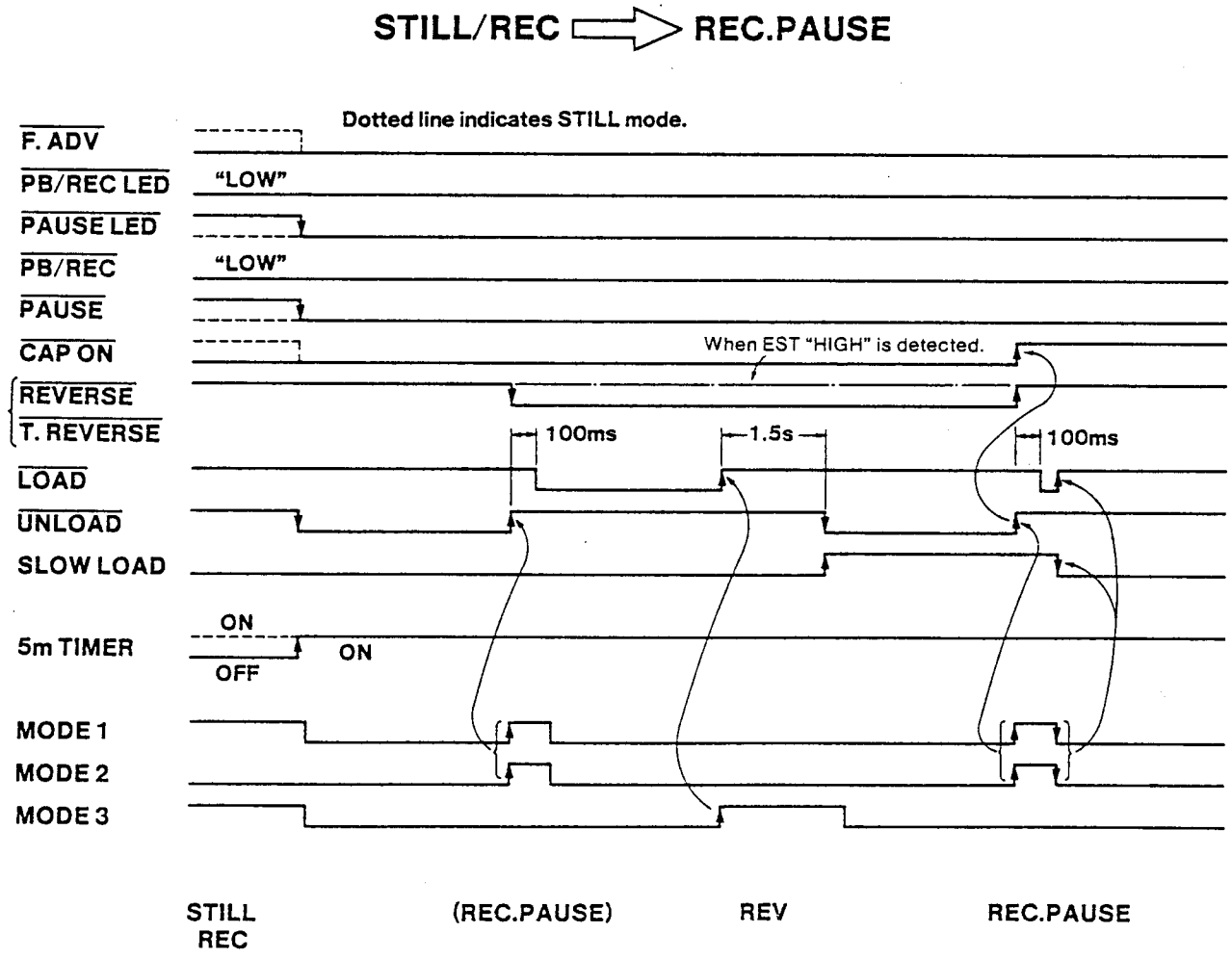


Fig. 2-2-15.

12) REC PAUSE — REC (See Fig. 2-2-16)

When the PAUSE button is pressed in the REC PAUSE mode, the set is returned to the REC mode.

a) The PAUSE LED is switched OFF and PAUSE is set to high. The ASR is set to high for 1.2s and the assemble record signal is output.

b) The capstan motor is driven in the forward direction (CW).

c) The loading motor loads slowly (CCW).

d) When the MODE SELECT SW position (1, 0, 1) is detected, the loading motor is stopped and the VCR is placed in the REC mode.

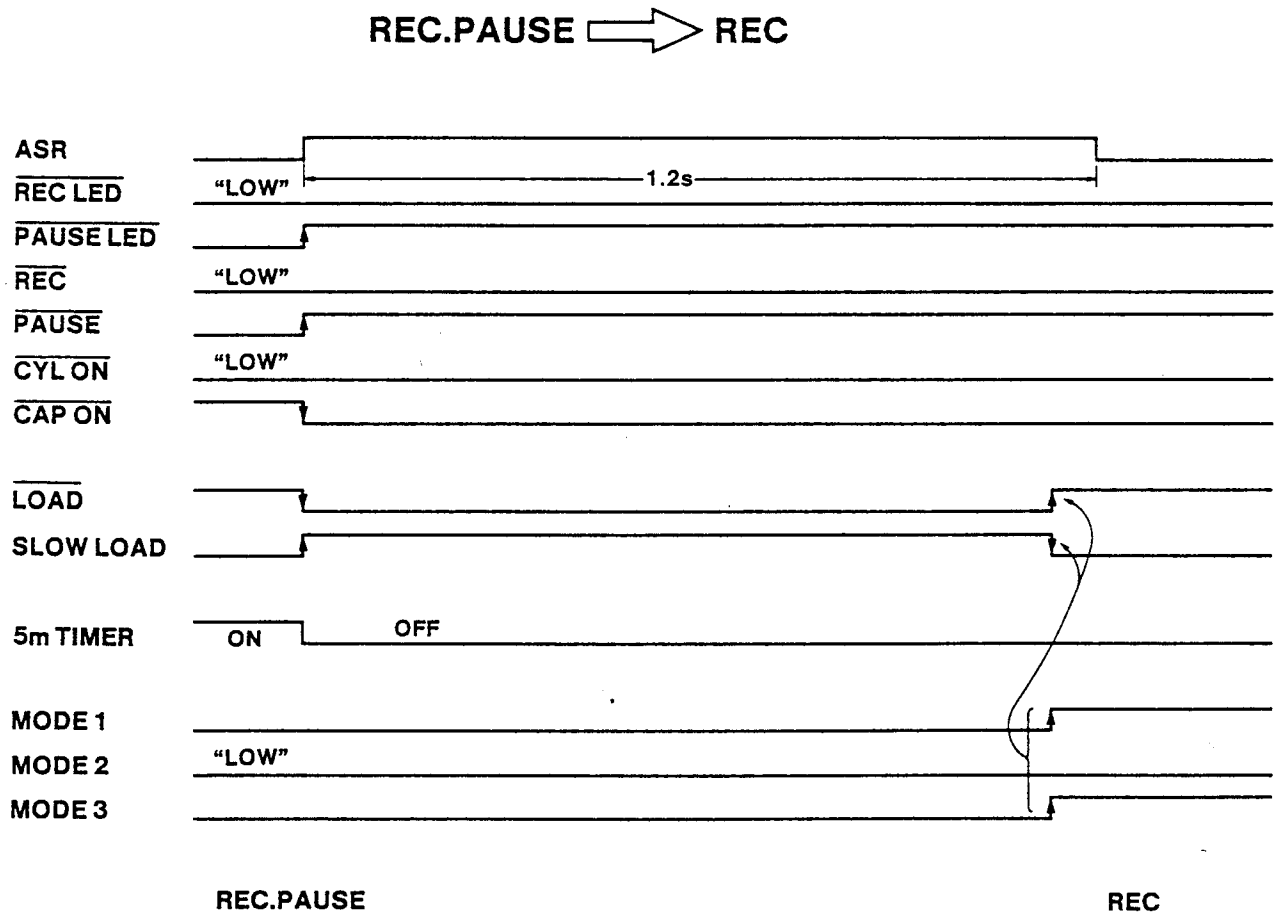


Fig. 2-2-16.

13) FRONT LOAD (See Fig. 2-2-17)

When the cassette is inserted:

a) The EED SW input changes from high to low.

b) The KEY DIS, F LOAD outputs are set to low, the front loading motor is driven in the CCW direction and the cassette holder is lowered.

c) When the cassette holder is lowered and the LSP SW input is set to high, the front loading motor drive is stopped and the LSP output is set to low.

d) When the CDT SW input becomes low, the TAPE IN LED lights up.

e) If the low CST SW input is not detected within 5 seconds, the cassette is automatically ejected.

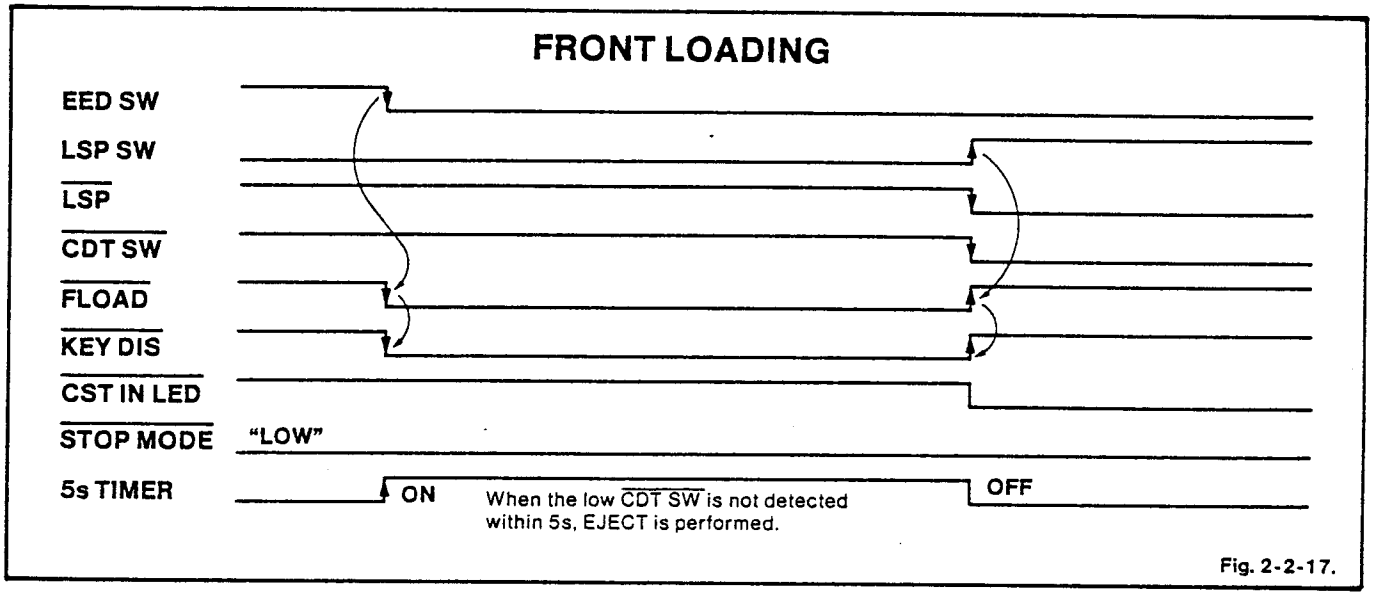


Fig. 2-2-17.

14) STOP → FF/REW (See Fig. 2-2-18)

a) When the FF (REW) button is pressed, the latch coil is switched ON, the loading motor loads (CCW) slowly for 200ms and the reel brake is disengaged and maintained in this condition.

b) CAP H is set to high and the capstan motor is driven in the forward direction (CW) [reverse (CCW) for REW] at maximum speed. At the same time, T REVERSE is set to high (low for REW).

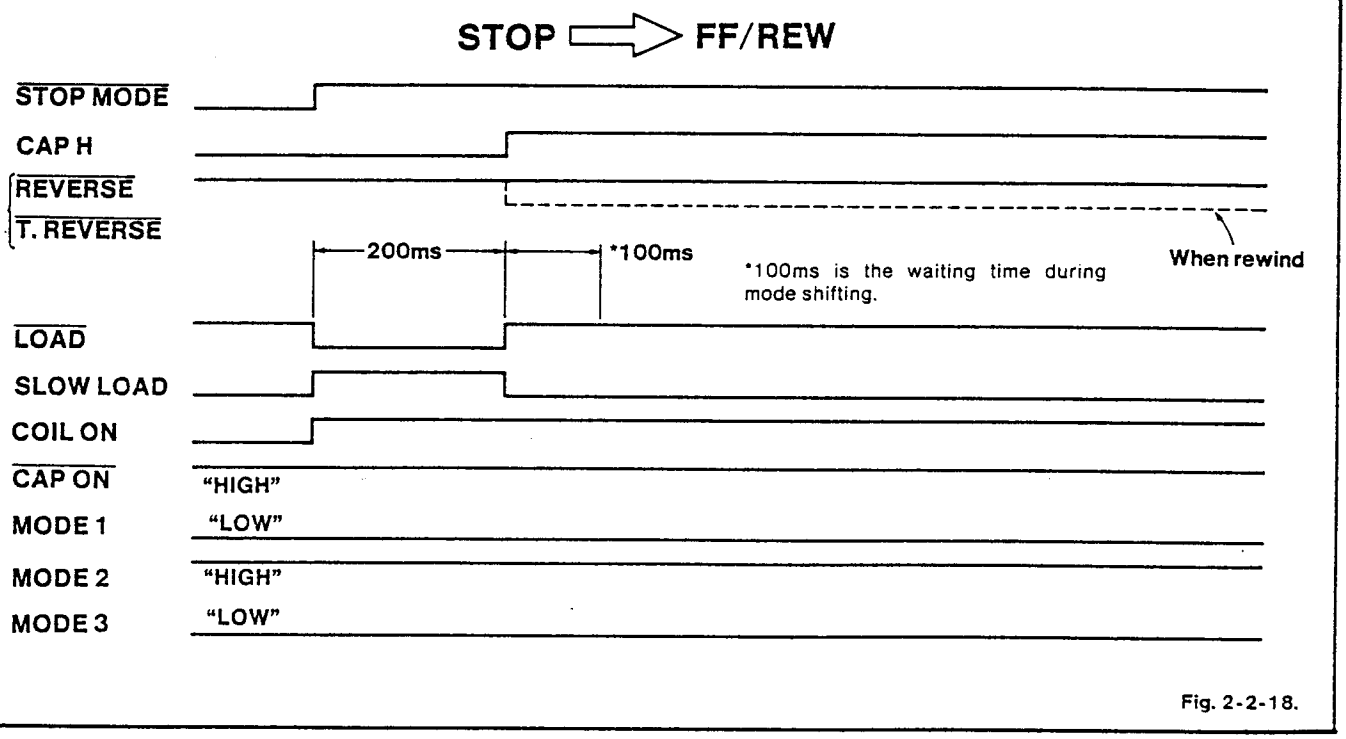


Fig. 2-2-18.

15) FF/REW — STOP (See Fig. 2-2-19)

When the STOP button is pressed in the FF/REW mode.

a) A reverse (CCW) signal is sent to the capstan motor [forward (CW) for REW] for 100ms and the brake is applied to the capstan motor.

b) CAP H is set to low and the capstan motor drive is stopped.

c) The latch coil is turned off; the loading motor unloads (CW) until the MODE SELECT SW position [(0, 1, 0) - (0, 0, 0)] is detected. With this operation, the brake is applied instantly to the reel.

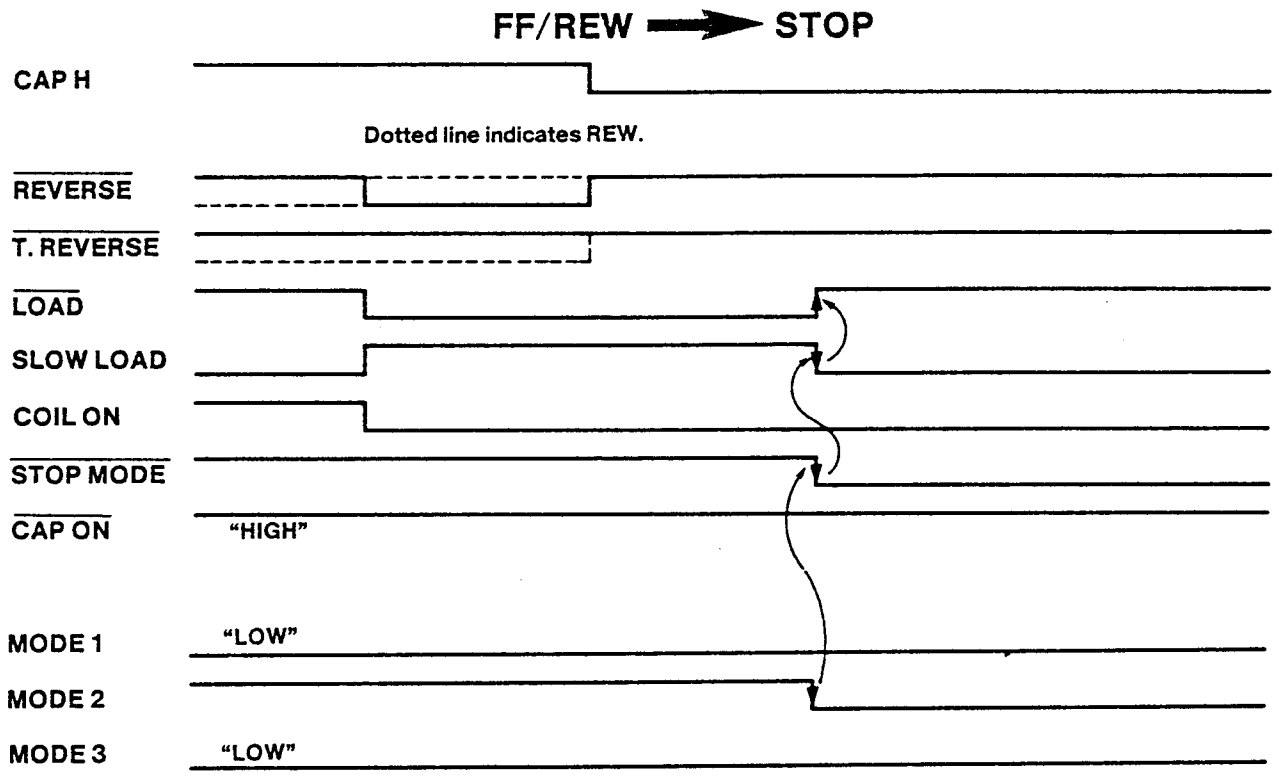


Fig. 2-2-19.

16) STOP — EJECT (See Fig. 2-2-20)

When the EJECT button is accepted:

a) A STOP PULSE (200ms, high) is output and the EJECT OUT low output and the KEY DIS output are set to low. (If the set was not in the STOP mode, this operation places the set in the STOP mode.)

b) If the STOP MODE signal is low, the latch coil is turned ON, the loading motor loads for 200ms and the reel brake is disengaged and maintained in this condition.

c) After 100ms, the capstan motor is driven slowly and tape slack is removed.

d) The front loading motor is driven in the CW direction and the tape is ejected.

e) When the cassette holder rises and the high EED SW input is detected, the latch coil is turned OFF. In addition, the SLOW LOAD, EJECT OUT outputs are set to high and the loading motor unloads slowly. At this time, brakes are applied to both reels.

f) When the MODE SELECT SW position [(0, 1, 0) - (0, 0, 0)] is detected, the capstan and loading motor drives are stopped, the STOP MODE output is set to low and the set is placed in the STOP mode.

Note: For operation e), if the high EED SW input is not detected within 5 seconds, the front loading motor is automatically stopped.

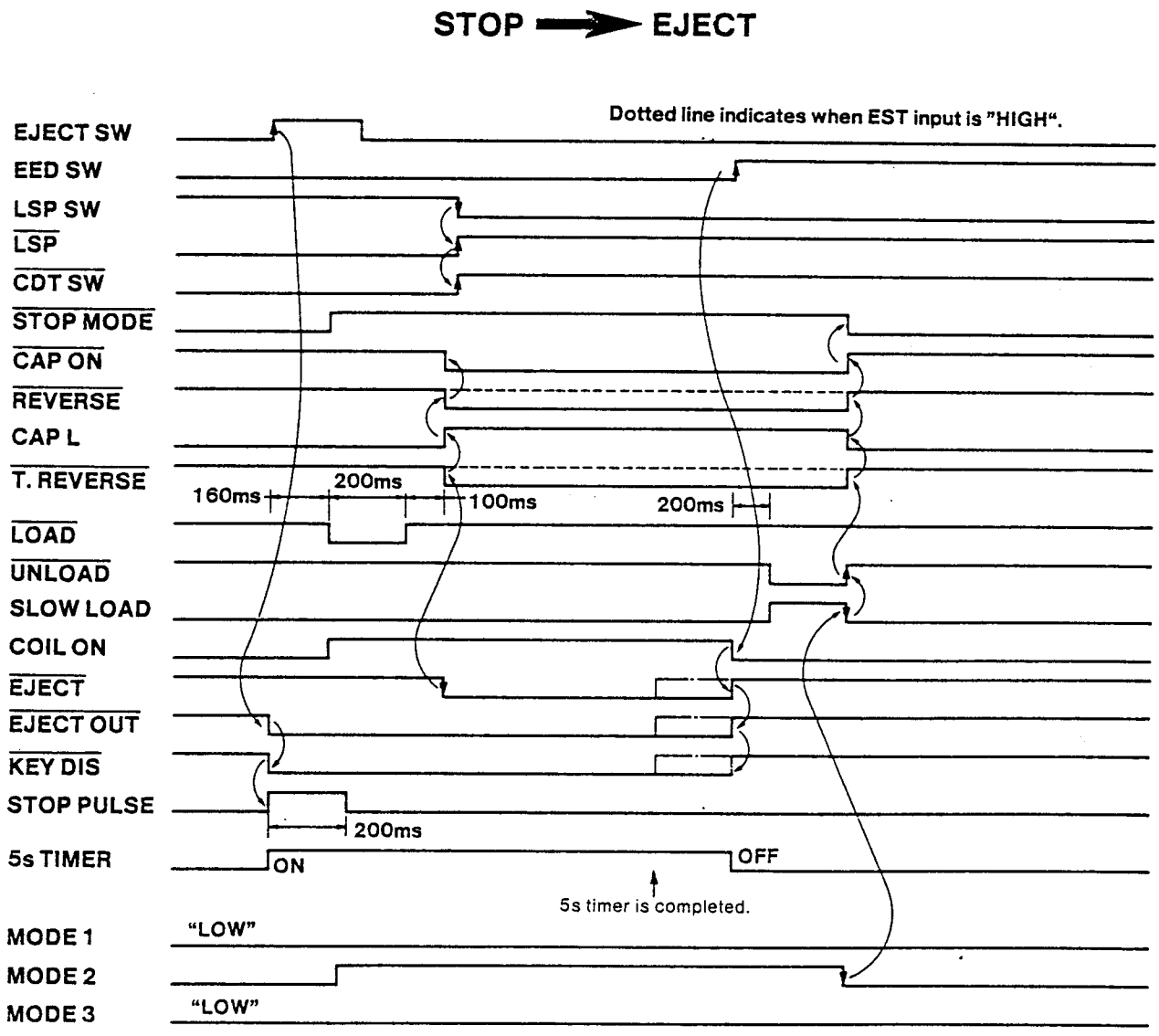


Fig. 2-2-20.

17) CHANGING TO THE NEXT MODE VIA THE STOP MODE

In the following cases, entry into the new mode is always executed via the STOP mode.

a) During PB/STILL/CUE/REVIEW, when the EJECT button is pressed.

b) During FF/REW, when the EJECT button is pressed.

c) During FF/REW when the PB button is pressed, or when the PB and REC buttons are pressed simultaneously.

d) During FF, when the REW button is pressed.

e) During REW, when the FF button is pressed.

18) During loading, when the FF/REW/EJECT button is pressed, the set moves into the next operation after completing loading.

Note: For items 17, 18, see the Mode Shift Chart.

INPUT KEY / MODE	STOP	PLAY	REC	PAUSE	FF	REW	EJECT
STOP	STOP	PLAY	REC	STOP PAUSE	FF	REW	EJECT
PLAY	STOP		REC	STILL	CUE	REV	STOP EJECT
REC	STOP			REC PAUSE			
STILL	STOP		REC PAUSE	PLAY	CUE	REV	STOP EJECT
REC PAUSE	STOP			REC			
STOP PAUSE	STOP	STILL	REC PAUSE	STOP	FF	REW	EJECT
CUE	STOP	PLAY				REV	EJECT
REV	STOP	PLAY			CUE		EJECT
FF	STOP	PLAY	REC			REW	EJECT
REW	STOP	PLAY	REC		FF		EJECT
LOADING	LOAD STOP	PLAY	REC	Accept-able	LOAD FF	LOAD REW	LOAD EJECT
UNLOADING	STOP	STOP PLAY	STOP REC	STOP PAUSE	STOP FF	STOP REW	STOP EJECT

Note:
LOAD STOP means shifting to STOP mode after loading.
STOP PLAY means shifting to STOP mode and then entry into PLAY mode.

Table 2-2-5.

2-2-6. OUTPUT SIGNALS IN STEADY STATE

Table 2-2-6 shows output signals in steady state.

MODE / OUTPUT	STOP	PLAY	REC	STOP PAUSE	STILL	REC PAUSE	CUE	REV	FF	REW	TIMER REC	FLOAD	EJECT	LOADING	UN-LOADING	DEW
PLAY OUT		○			○		○	○						△		
REC OUT			○			○					○			△		
PAUSE OUT					○	○										
F. ADV. OUT																
LOAD OUT														○		
CYL ON		○	○		○	○	○	○			○			○		
C. DRIVE		○	○		Pulse		○	○			○		○	○	○	
PLAY LED		○	○		○	○	○	○			○			△		
REC LED			○			○					○			△		
PAUSE LED				○	○	○								△		
DEW LED																Flashing
F LOAD												○				
EJECT													○			
EJECT OUT													○		△	
KEY DIS												○	○		△	
SEARCH							○	○								
REVERSE						◎		○		○			○		○	
LOAD														○		
UNLOAD															○	
SLOW LOAD*						◎		◎	◎	◎			◎		◎	
COIL ON*									○	○			○		○	
CAP HI*									○	○						
CAP LO*													○		○	
T. REVERSE						◎		○		○			◎	◎	○	
PWR CONT	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	△
STOP MODE	○			○								○				○

Table 2-2-6.

NOTES:
1. ○ mark indicates the active condition.
2. * mark indicates HIGH ACTIVE, other are LOW ACTIVE.
3. ◎ mark indicates transitional output signals.
4. △ mark indicates high or low depending on the mode.
5. Blanks indicate the NON ACTIVE status.

2-3. SERVO CIRCUIT

2-3-1. SERVO CIRCUIT COMPOSITION

The servo circuit is basically composed of IC703, IC803, IC805, IC804, and the cylinder and capstan motors. The block diagram for the servo circuit is shown in Fig. 2-3-1.

IC703 is used for phase control of the cylinder and capstan motors. IC703 also includes the circuit for frequency division of the chroma frequency (fsc) to produce the reference signal, the frequency division circuit for V SYNCH and CAP FG, the circuit for generating the HEAD SW signal from the PG pulse, and the circuit which compares these signals and outputs phase errors.

IC803 and IC804 each contain two circuits. One is for making the F/V conversion of the respective cylinder and capstan FG signals. (These converted signals are output as speed errors, via the speed control circuits.) The other is for mixing the phase errors and the speed errors, outputting the resulting signals as the cylinder and capstan motor control signals.

IC805 is used for cylinder motor drive, and a 3 phase signal is generated for driving the cylinder motor. The capstan motor has a built-in motor drive IC which operates the same way as IC805.

1. RECORDING

The conditions pertaining to the servo system required to record video signals, which have been converted to enable recording onto a magnetic tape field by field (pulse by pulse of the vertical sync signal) are as follows: first, the speed and phase of the capstan motor must be controlled so that the supply speed of the tape is made constant, and second, the speed and phase of the cylinder motor must be controlled in order to synchronize the rotations of the cylinder with the vertical sync signal in the video signals which are to be recorded. (Refer to Fig. 2-3-2)

2. PLAYBACK

So that the video heads are able to trace the already recorded video tracks faithfully during playback, the speed and phase of the capstan motor are controlled with the CTL (control) signal already recorded on the magnetic tape and the PG signal of the cylinder position signal. These signals act as references. (Refer to Fig. 2-3-3)

3. FAST FORWARD AND REWIND

Fast forward is executed by rotating the capstan motor at high speed in the clockwise direction, and rewind in the counterclockwise direction. Fast forward and rewind operations are controlled with two signals. One is the CAP H signal to rotate the capstan motor at high speed, and other is the F/R signal to decide the direction of the capstan motor rotation.

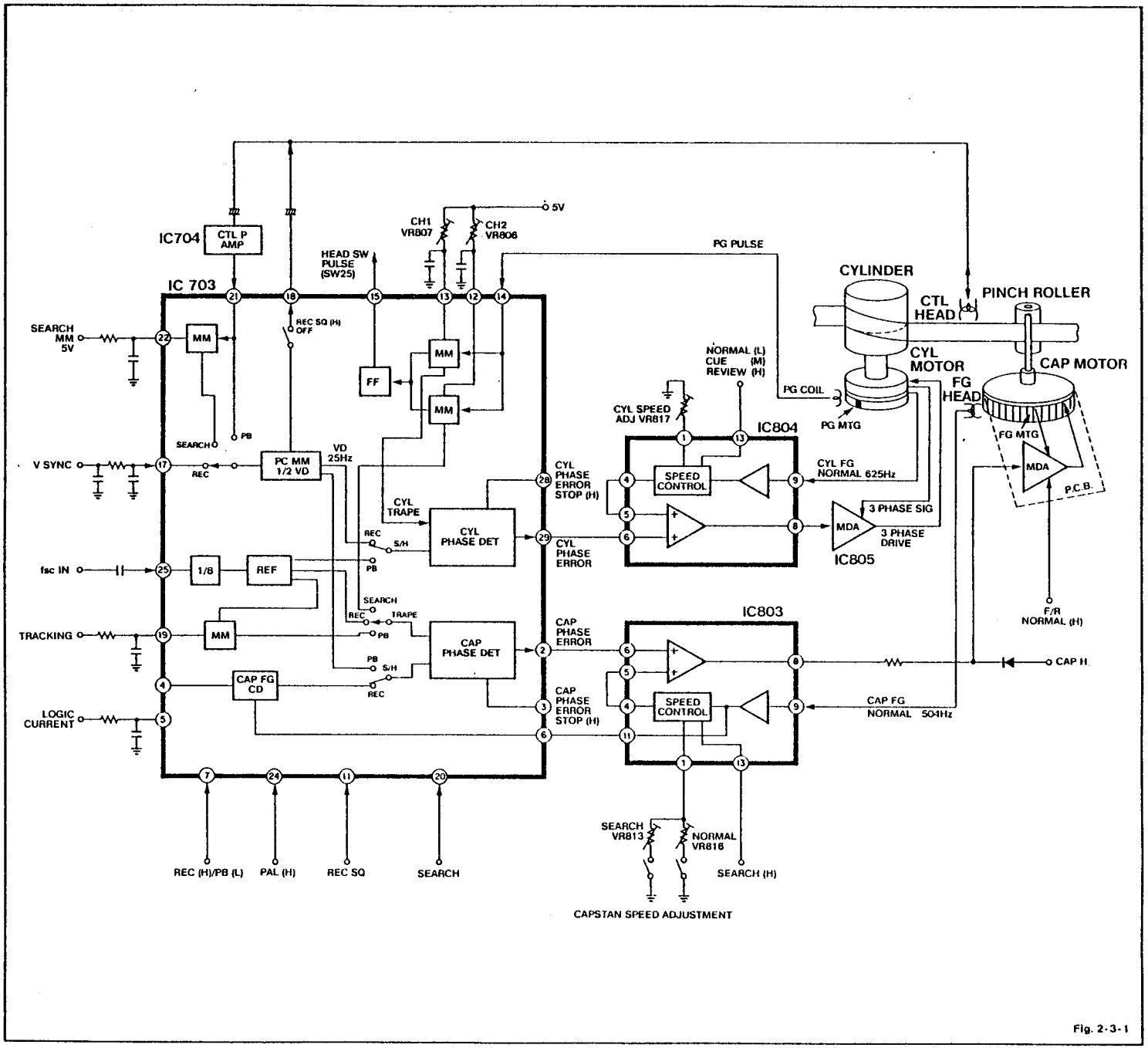


Fig. 2-3-1

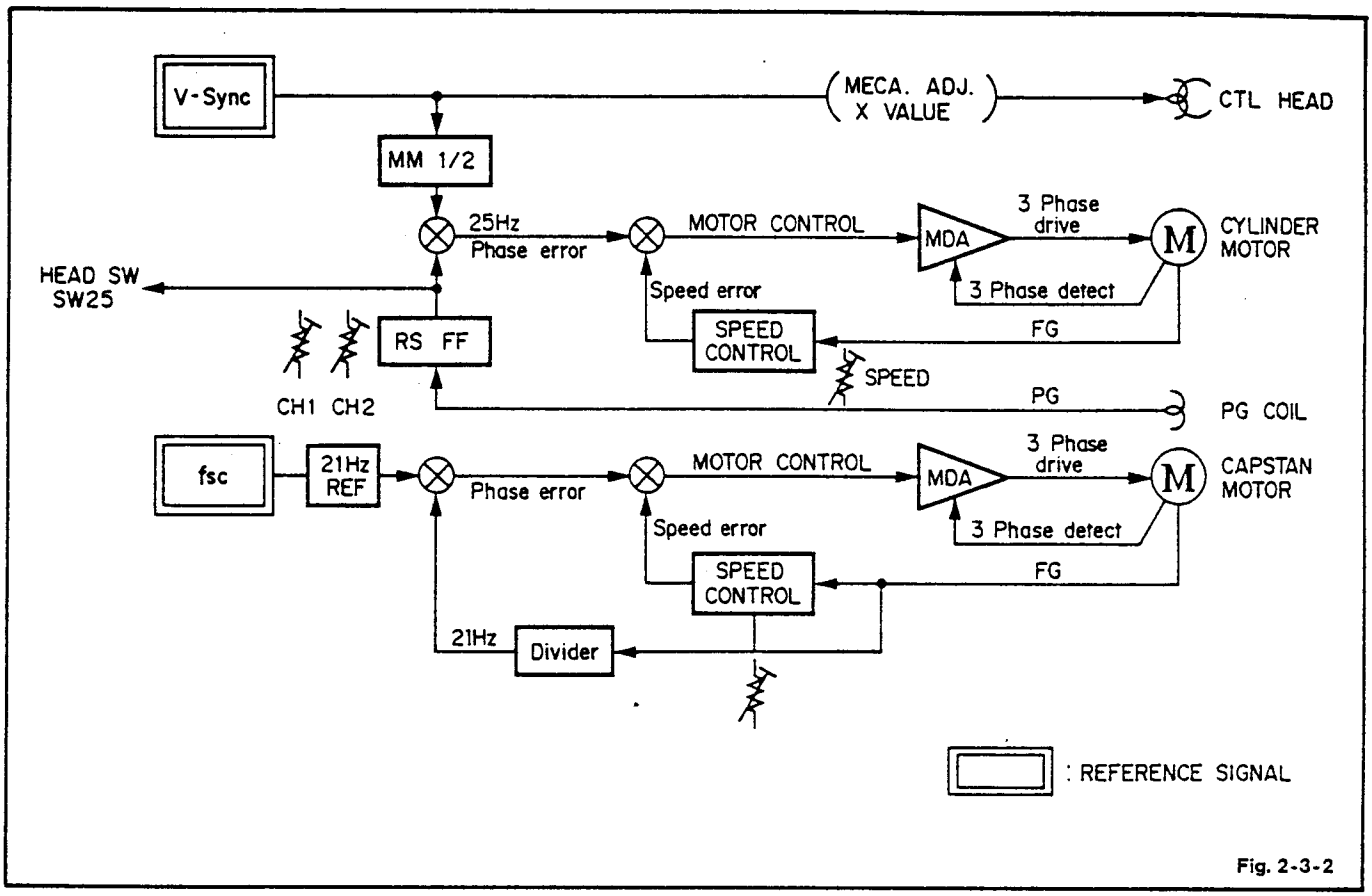


Fig. 2-3-2

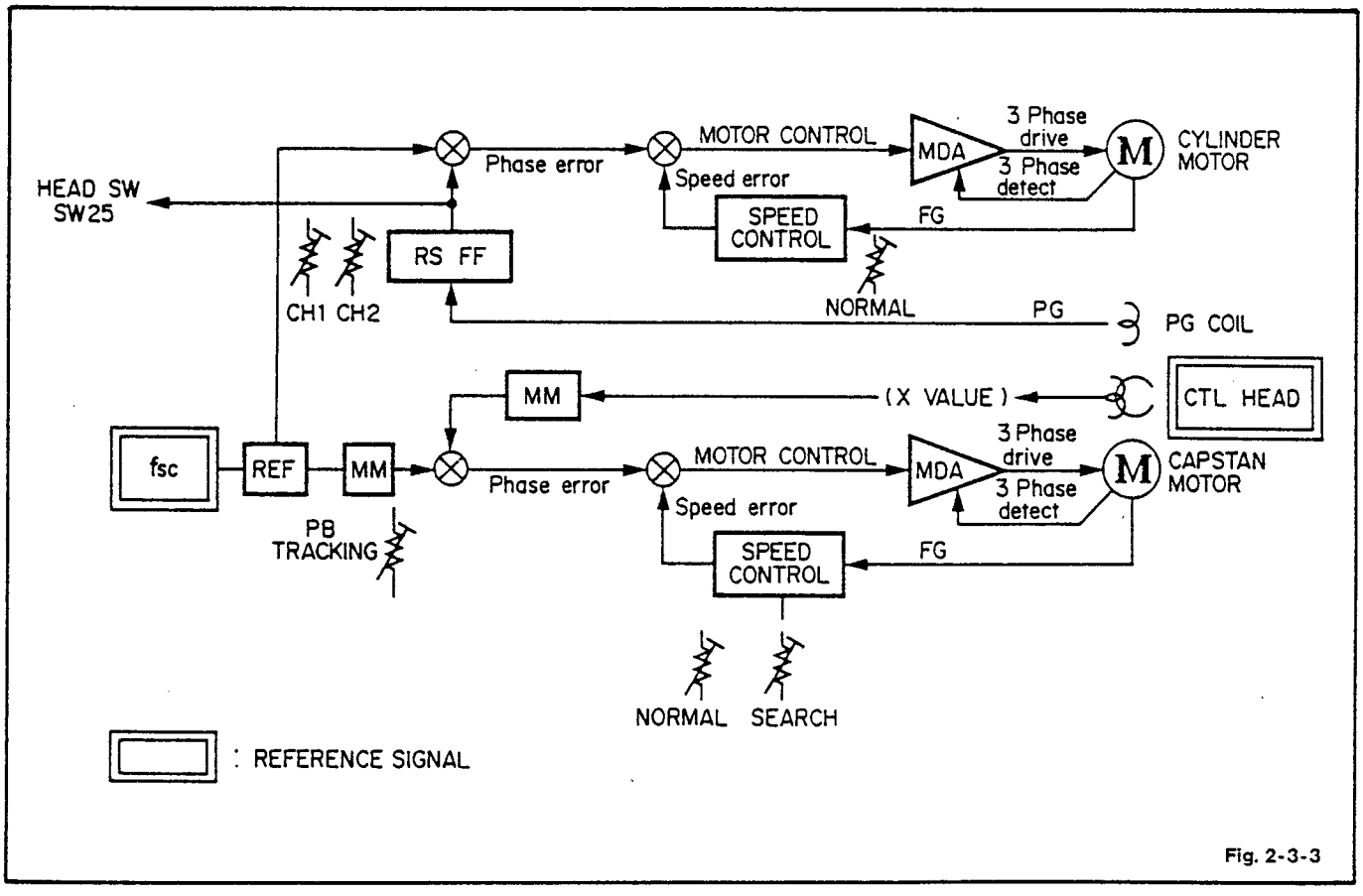


Fig. 2-3-3

2-3-2. SPECIAL VARIABLE SPEED PLAYBACK

"Special playback" refers to playing back a tape at a different speed from that used during recording. This unit accepts the special variable speed playback mode. Table 2-3-1 gives the rotational speed of the cylinder and tape forwarding speeds during the special playback mode.

The tape speed is varied by changing mainly the capstan rotational speed (= the tape speed). When the capstan speed is changed during the search mode (CUE/REVIEW), the cylinder rotational speed is varied simultaneously. During REVIEW and CUE the cylinder speed is set to 1457 rpm for review and 1529 rpm for cue mode (the writing speed of the tape). The frames are advanced at about 5 times than that of normal playback speed.

When recorded pictures are played back at a different speed, the noise components increase at the minimum end area of the envelope shown in Fig. 2-3-4. The number of horizontal sync. signals differ between channel 1 (CH1) and channel 2 (CH2) or the vertical sync. signal becomes indistinct in each channel so that the picture becomes unstable. In order to safeguard against picture rolling, a dummy vertical sync. pulse (the additional pulse) is created and this is added to the playback video signal within 6.5H to the leading or trailing edge of the head switching pulse (SW25).

The variable speed is controlled as follows: the additional V sync pulse, being supplied so that the picture does not roll at irregular synchronization, follows the top of the picture so that the noise band is not made conspicuous.

Mode	Tape Speed	Cylinder speed	Playback speed (multiple recording speed)
STILL		1500rpm	0
REVIEW	Approx. 117mm/sec	Approx. 1457rpm	Approx. 5
CUE	Approx. 117mm/sec	Approx. 1529rpm	Approx. 5

Table 2-3-1.

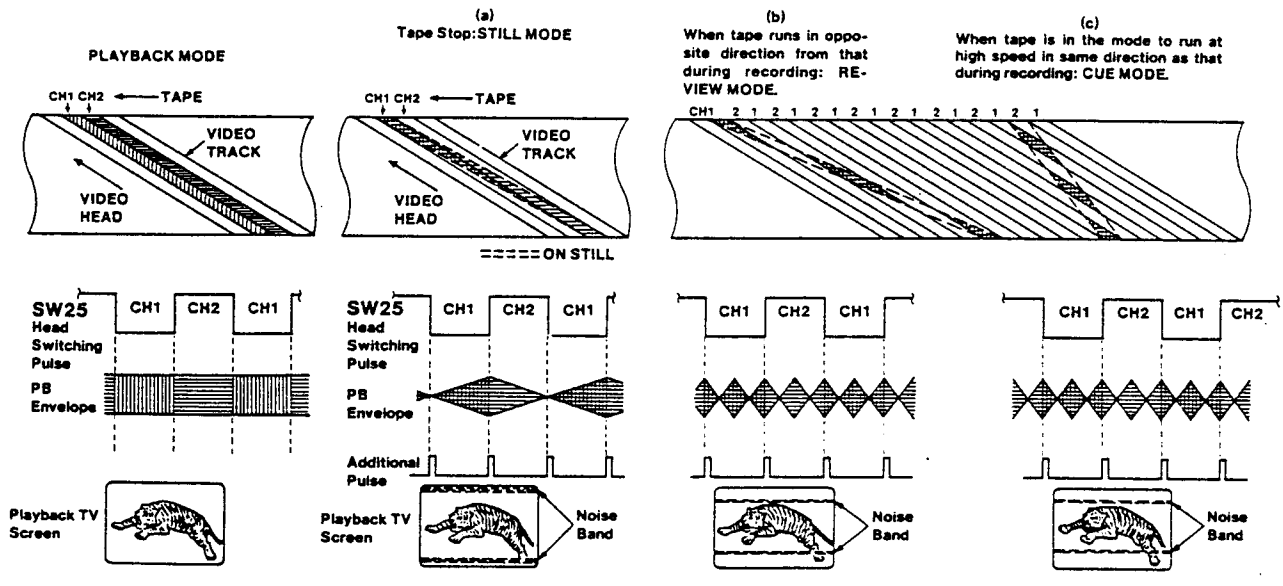


Fig. 2-3-4

2-3-3. SERVO CIRCUIT OPERATION

1. CYLINDER SPEED CONTROL

Cylinder speed control is executed by IC804 and its peripheral circuits. During recording, the cylinder speed is maintained at a constant speed of 1500 rpm. During playback, the cylinder speed is compensated only in the CUE and REVIEW modes.
This prevents horizontal sync loss by deviation of the horizontal frequency because of the changing relative speed of the V HEAD, as the playback tape speed for CUE or REVIEW is approximately 5 times faster than the recording tape speed.

Fig. 2-3-5 shows the block diagram for the cylinder speed control circuit. The FG pulse is taken from the cylinder motor, input on pin 9 of IC804, and a sample pulse is generated by its passage through the amplifier. This pulse is used for sample hold for the sawtooth wave. The speed is controlled by the VR connected to pin 1, and the speed error is output on pin 4 of IC804.
Cylinder speed compensation in CUE and REVIEW modes is executed by the tri-state input on pin 13 of IC804.

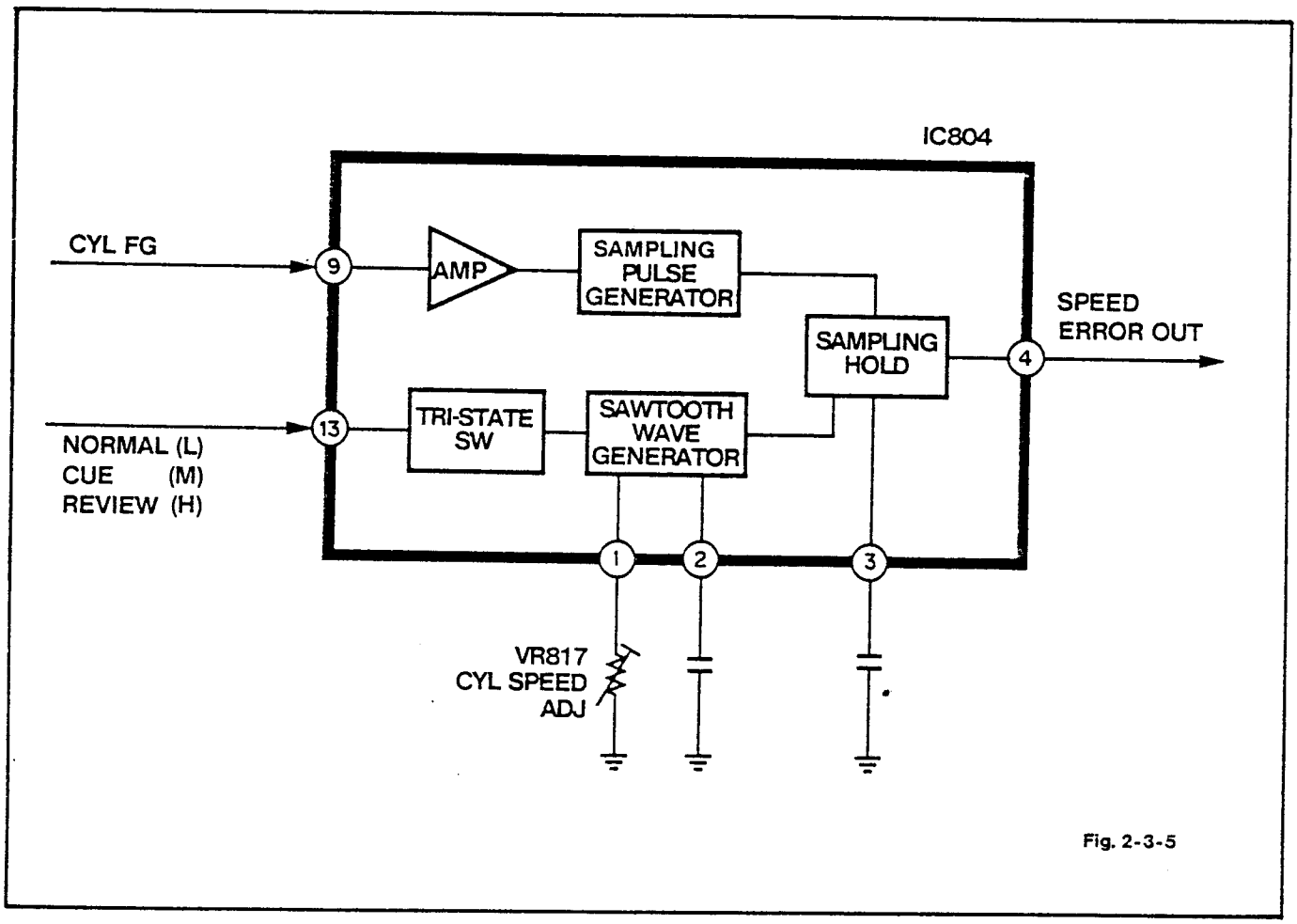


Fig. 2-3-5

2. CYLINDER PHASE CONTROL

Cylinder phase control is executed by IC701 and its peripheral circuits.

During recording, phase control is used to decide the positional relationship between the video signal and the magnetic tape on which it is to be recorded. Adjustment is made to preserve this relationship so that the time relation of 6.5H (6.5 horizontal synch signals, 64 μsec x 6.5 = 416 μsec) $\pm$ 0.5H is maintained between the leading edge of the vertical sync signal (at the time of switching from Ch 2 to Ch 1) and the head switching signal.
Fig. 2-3-6 shows the block diagram for the cylinder phase control circuit during recording, and Fig. 2-3-7 shows the timing chart for this.

CYL PG passes through the monostable multivibrators of CH1 and CH2, compensates for the deviation of the PG magnet mounting position, and produces the head switching pulse. PHASE DET compares the VD25 signal (from division of V.SYNC in half) and the CH1 MM output and outputs the phase error.
At this time, the relation between the head switching pulse and V.SYNC is 6.5H by internal setting in the IC.
For the phase control during playback, the video head rotation phase is controlled so that both the CH1 video head can track accurately the CH1 track (on which the video signal is recorded) and the CH2 video head can track accurately the CH2 track.

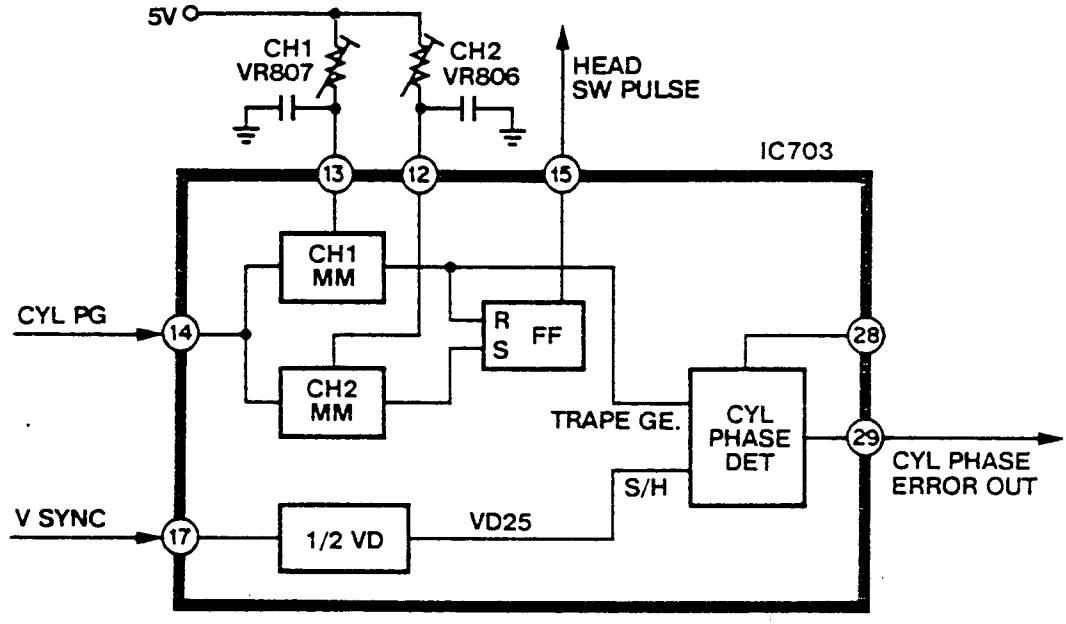


Fig. 2-3-6

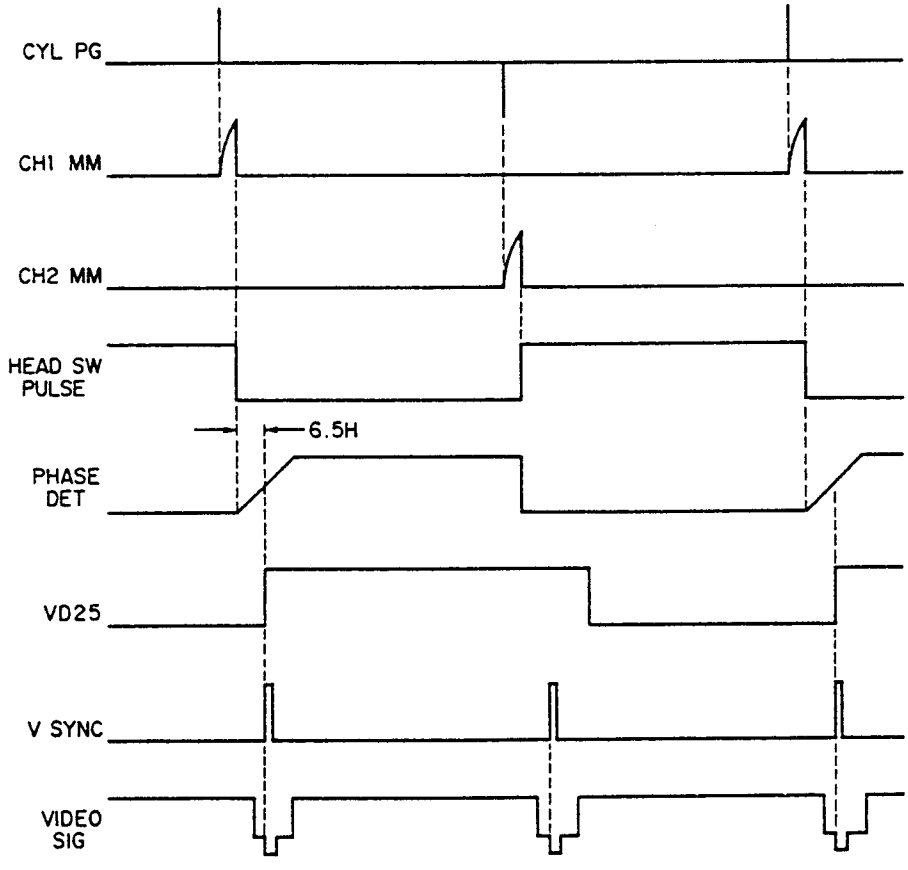


Fig. 2-3-7

Fig. 2-3-8 shows the block diagram for the cylinder phase control circuit during playback, and Fig. 2-3-9 shows the timing chart for this.

CYL PG passes through the monostable multivibrator circuits of CH1 and CH2 and produces the head switching pulse.

At this time, the monostable multivibrator circuits are controlled so that the relation for the already recorded V.SYNC signal becomes 6.5H, the same as during recording.

Furthermore, adjustment is executed by changing the time constant of the monostable multivibrator circuit because the head mounting position for using SP is different from the position for using LP.

During CUE and REVIEW, pin 28 of IC701 is made HIGH to stop the phase error, so that the cylinder speed can be compensated.

3. CAPSTAN SPEED CONTROL

Capstan speed is controlled to the constant speed in each mode by IC803 and peripheral circuits. During recording, the tape speed is controlled to the constant speed of 23.39mm/sec, and during playback, it is controlled to the normal speed of 5 times of CUE and REVIEW modes.

Fig. 2-3-10 shows the block diagram for the capstan speed control circuit. The FG pulse from the capstan motor is input on pin 9 of IC803, and passes through the amplifier to produce the sample pulse. This pulse is used for sample hold for the sawtooth wave. And the speed error is output on pin 4 of IC803.

At this time, the speed is controlled by changing the slope of the sawtooth wave with the VR connected to pin 1 of IC803.

Each speed signal is fed to pin 13 and the speed mode is selected by tristate circuit in the IC.

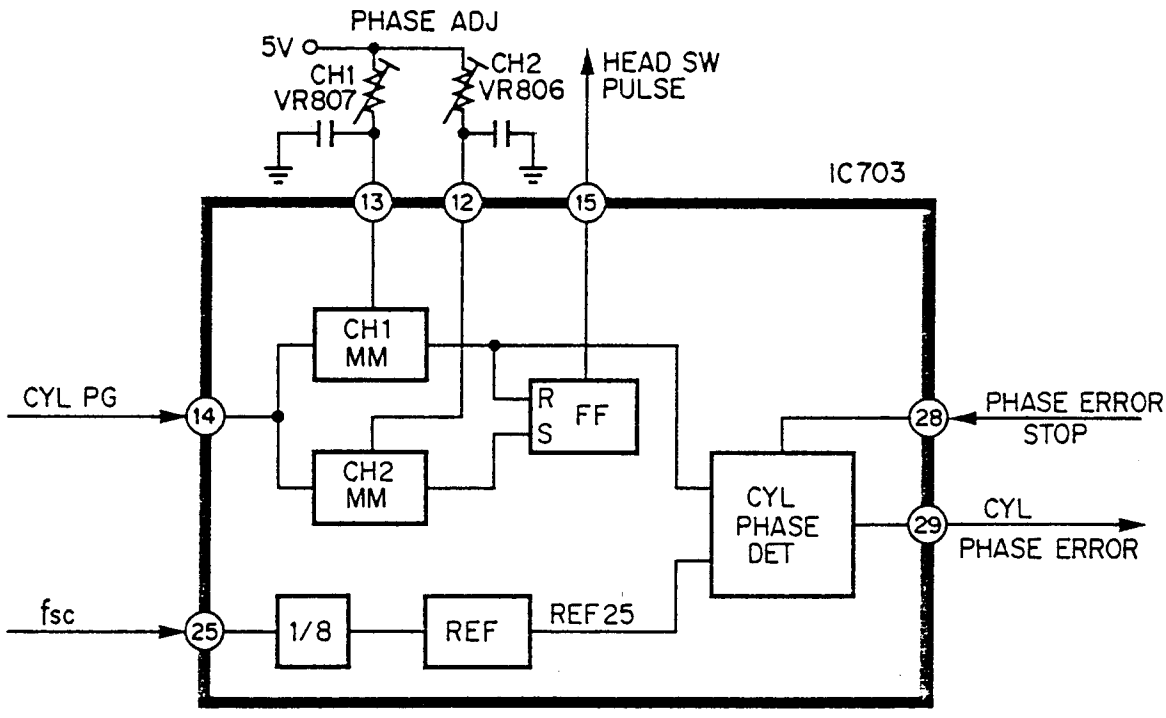


Fig. 2-3-8

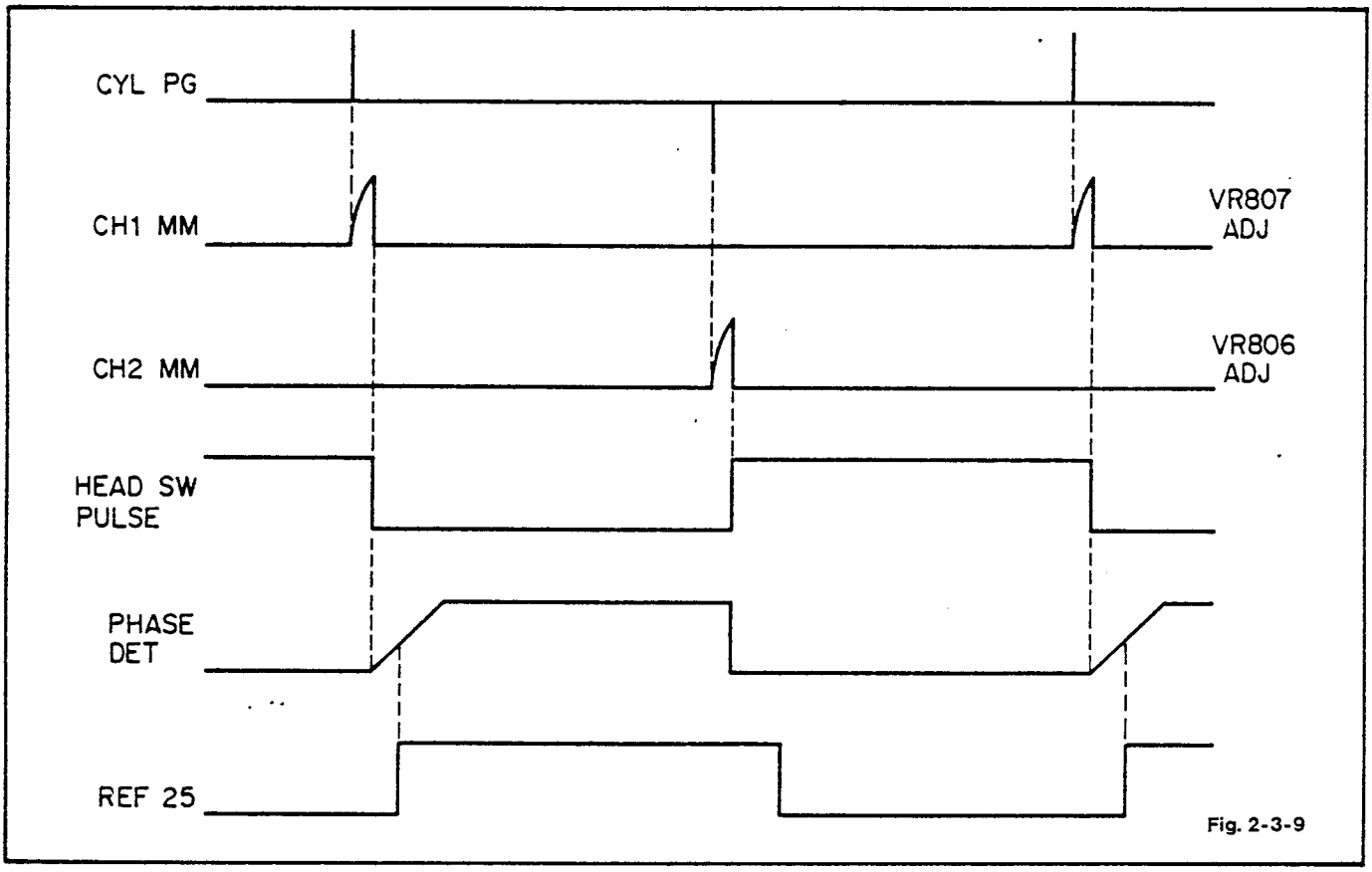


Fig. 2-3-9

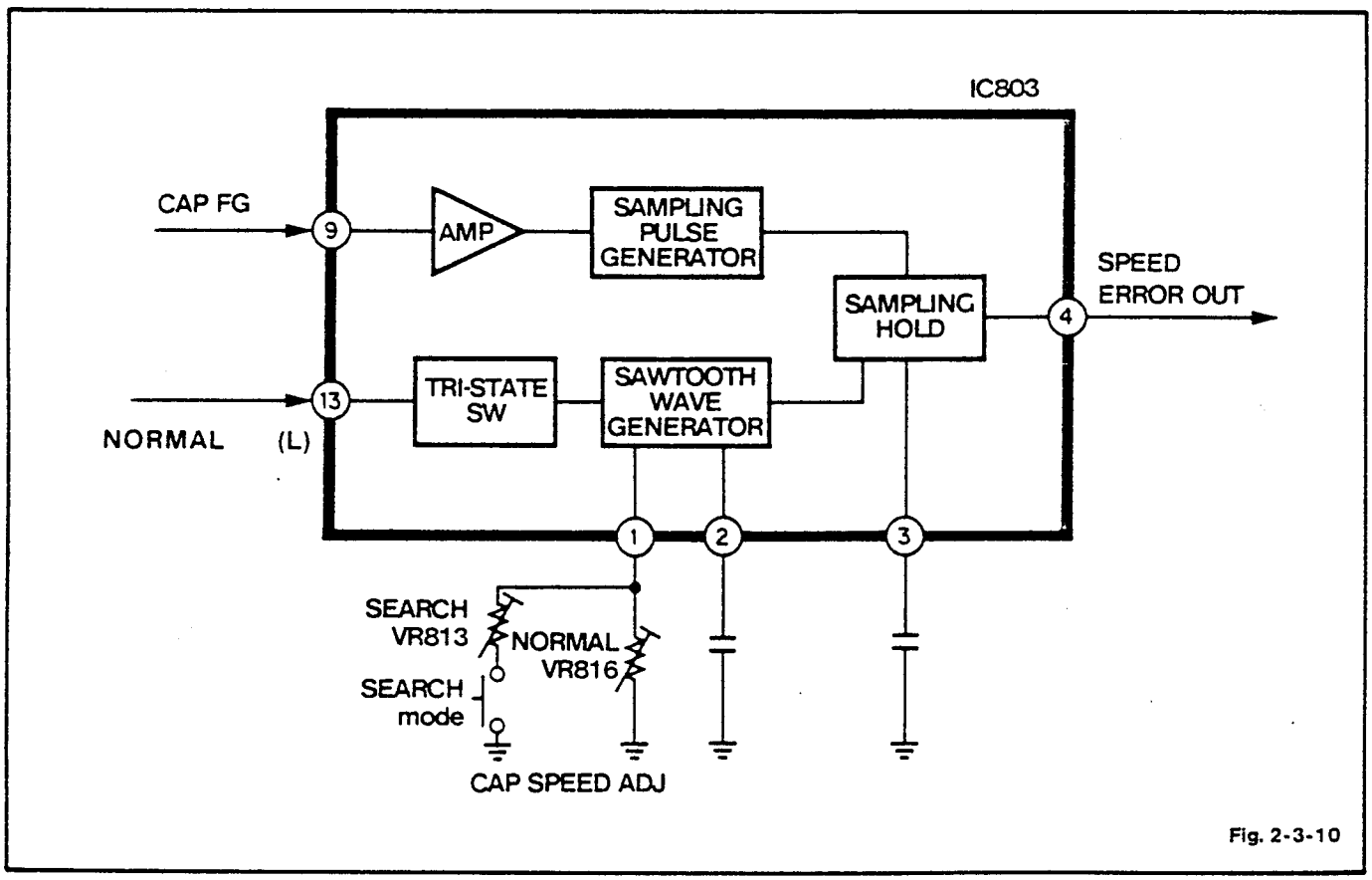


Fig. 2-3-10

4. CAPSTAN PHASE CONTROL

Capstan phase control is executed by IC703 and its peripheral circuits to keep the tape speed constant.
Fig. 2-3-11 shows the block diagram for the capstan phase control circuit during recording, and Fig. 2-3-12 shows the timing chart.
CFG25 is produced by frequency division of CAP FG. PHASE DET compares this with REF25, obtained by frequency division of fsc, and a PHASE ERROR signal is output.

During playback, the already recorded CTL PULSE is used as a reference, and the tape speed is controlled as required for NORMAL, CUE and REVIEW modes respectively. The cylinder rotation phase and the capstan rotation phase are synchronized by means of REF25 so that the CH1 video head can track accurately the CH1 track (on which the video signal is recorded) and the CH2 video head can track accurately the CH2 track.

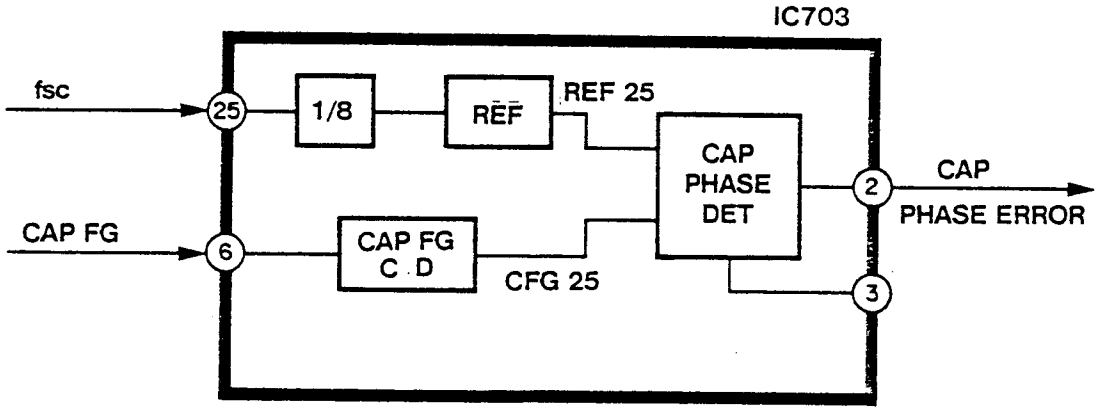


Fig. 2-3-11

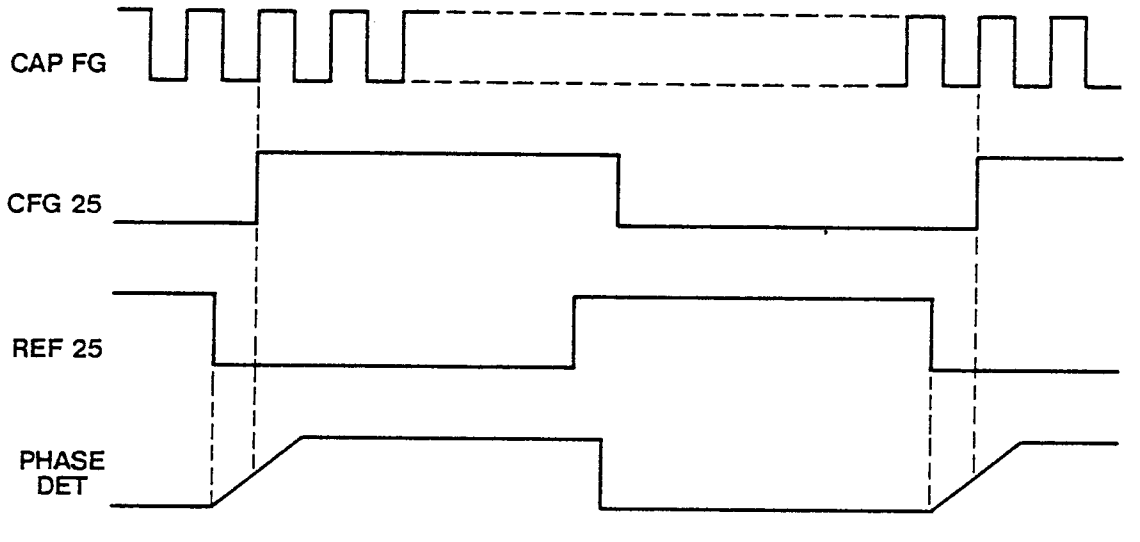


Fig. 2-3-12

Fig. 2-3-13 shows the block diagram for the capstan phase control during playback, and Fig. 2-3-14 shows the timing chart.
The CTL25 pulse is obtained by dividing the frequency of CTL.P in half and REF25 is compared by PHASE DET, and a PHASE ERROR signal is output. At this time, tracking adjustment is executed by delaying REF25 through the monostable multivibrator circuit.

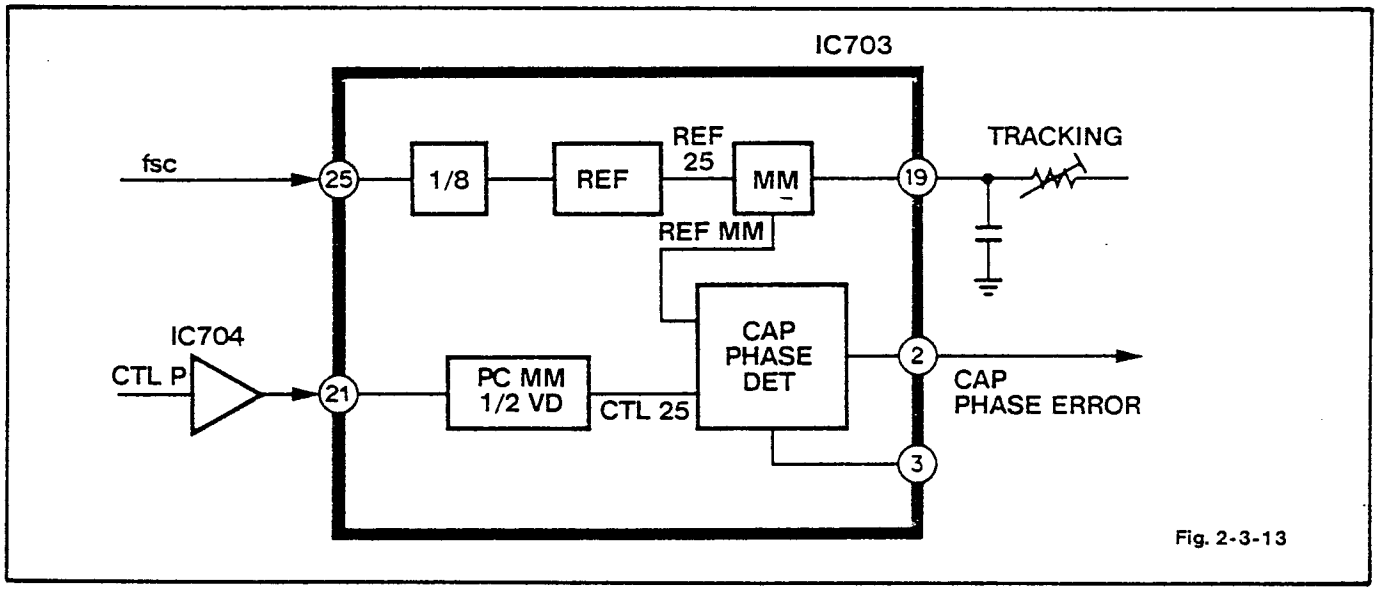


Fig. 2-3-13

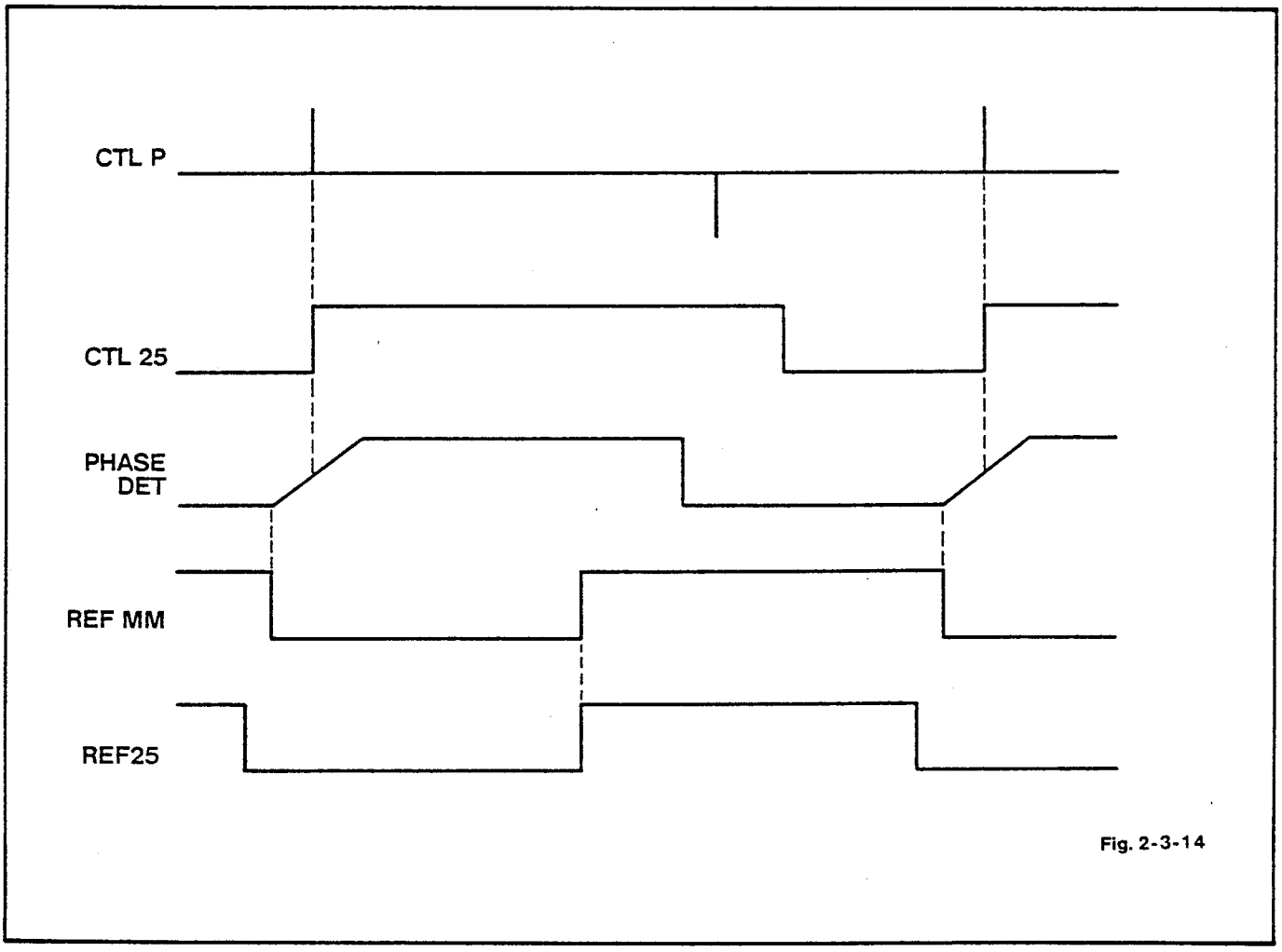


Fig. 2-3-14

5. ASSEMBLE RECORDING

The assemble recording method is used to eliminate the unrecorded portion on the tape at the junction between an already recorded frame and the frame to be recorded. When the PAUSE button is pressed in the record mode, the tape is rewound slightly to eliminate the unrecorded portion. When the PAUSE button is released, the CTL PULSE already recorded on the tape is synchronized with the V-SYNC of the video signal. At this time, the ASR (Assemble Record) signal is output from IC503 as a control signal.

The ASR signal is branched into three directions and executes three functions.

1. One of these signals goes via PV521 pin 1 (REC START) to the video circuit and cuts the recording signal.
2. The second goes to IC703 pin 9 and activates the Phase Control to synchronize the phase of the already recorded CTL PULSE and the V-Sync to be recorded. While synchronizing, one REV pulse is output from IC703 pin 8 to brake the capstan motor and assist the phase control function.
3. The third goes to IC703 pin 11 and cuts the REC CTL-PULSE.

The recording is started after the three functions described above are executed. As a result, a recording with no unrecorded portions and no joints between frames is obtained, with no noticeable distortion appearing on the screen.

The timing chart and its peripheral circuit are shown in Figs. 2-3-15 and 2-3-16.

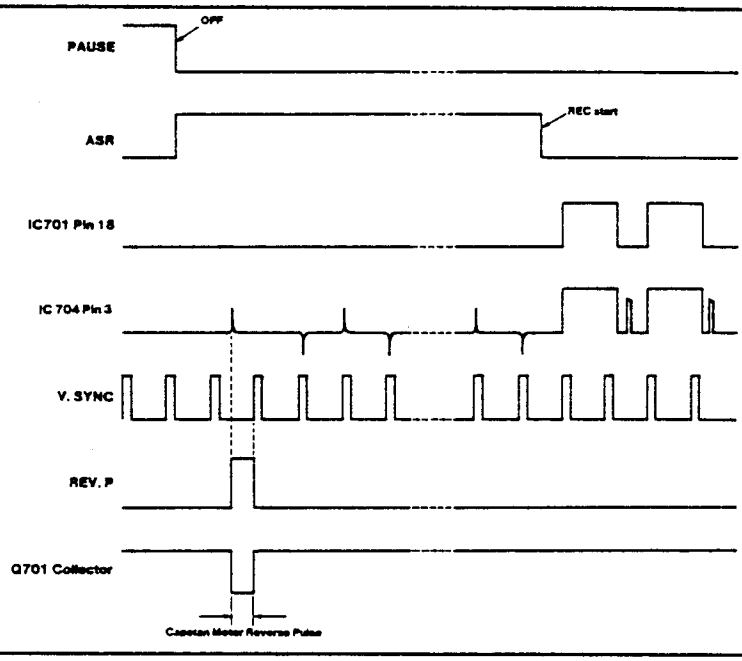


Fig. 2-3-15

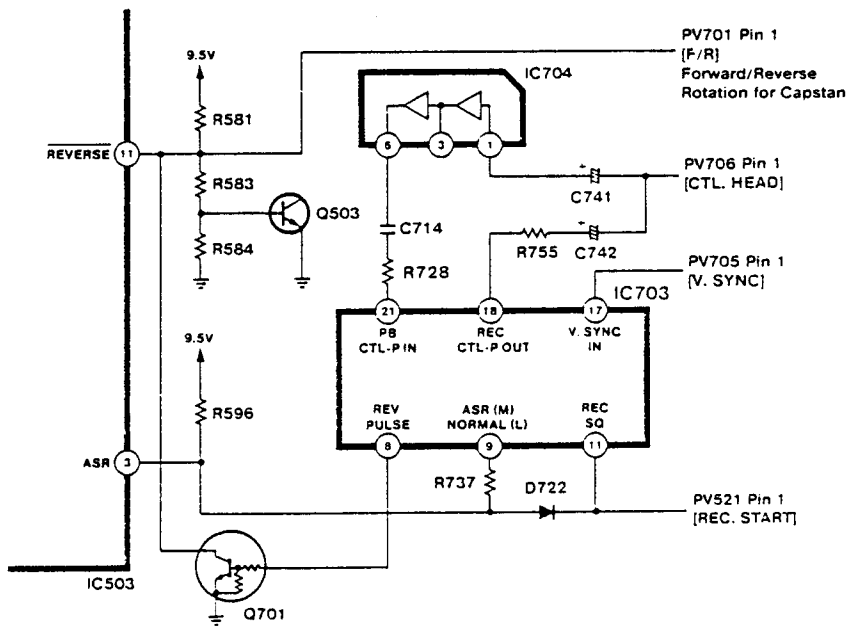


Fig. 2-3-16

6. CYLINDER AND CAPSTAN MOTOR DRIVE

Cylinder motor drive is executed by IC805 and its peripheral circuits.
Fig. 2-3-17 shows the block diagram for the cylinder motor drive.
The output of the Hall element installed on the stator of the cylinder motor is used for rotor position detection, and the generation of three-phase pulses. These are amplified in the driver part, and drive current flows to the stator coil. At this time, the motor speed is controlled by comparing the drive current feedback (by means of the feedback resistance) with the control signal.
The capstan motor has a built-in drive circuit.
The operation is the same as for the cylinder motor drive, but the F/R terminal is used in REVIEW and REC PAUSE for reverse running.

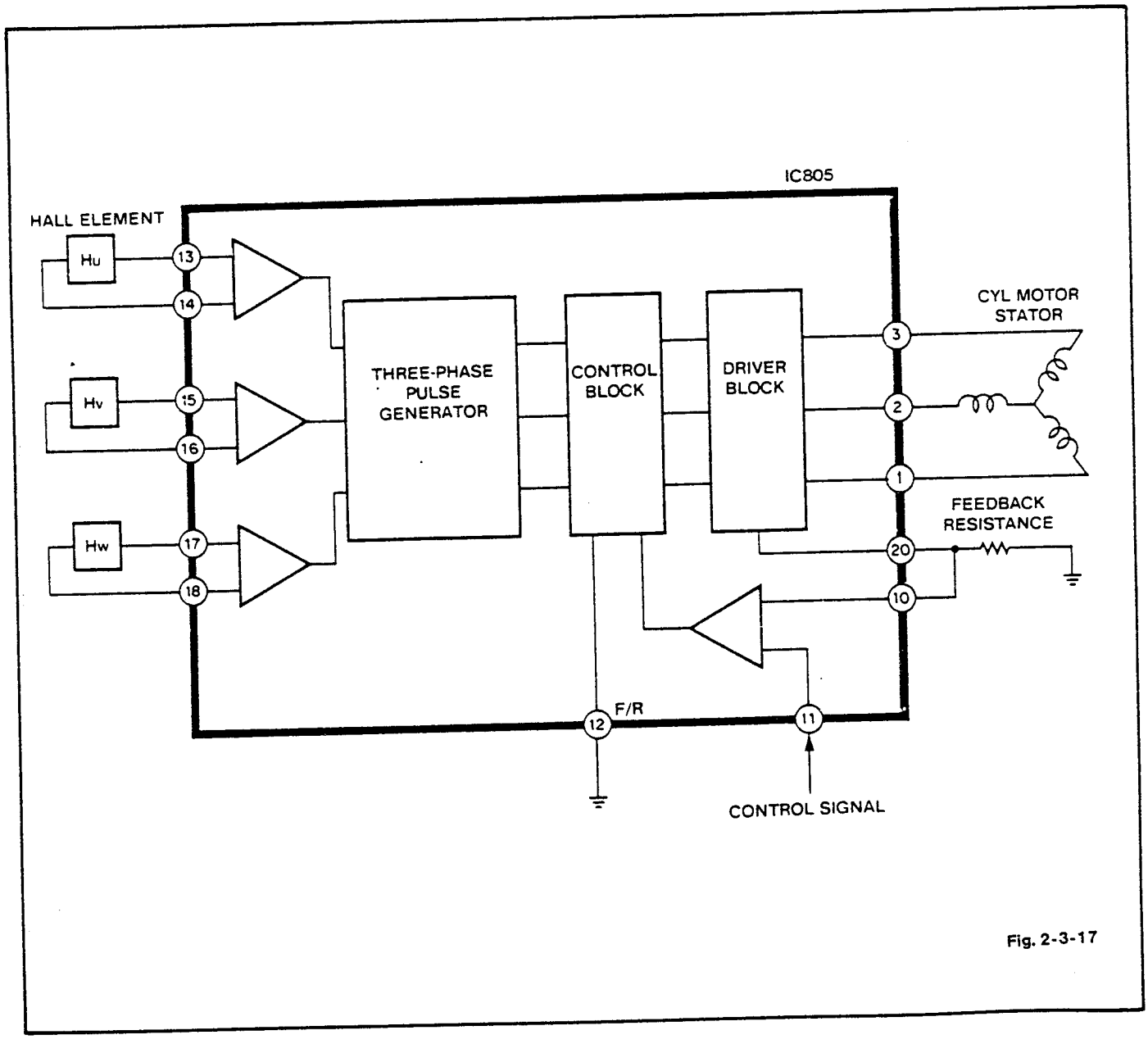


Fig. 2-3-17

2-3-4. STILL CIRCUIT

STILL PICTURE

In the playback pause mode, the tape stops running, and since CH1 and CH2 shown in Fig. 2-3-18 are overlapped and traced, a still picture is obtained.

To advance to the next frame, the capstan motor is rotated to the optimum position of the next frame. The following two signals are compared to stop this motor at the optimum position:

Head switching signal (SW25)
AGC signal

Actually, the video signals recorded onto the tape are superimposed at the beginning and end of each channel (overlap). During playback, switching is performed by the head switching signal (SW25) so that the CH1 and CH2 switching joints do not stand out and the playback signals are mixed.

The optimum timing for the switching is 6.5H (416μs) ahead of the leading edge of the vertical sync signal for each channel.

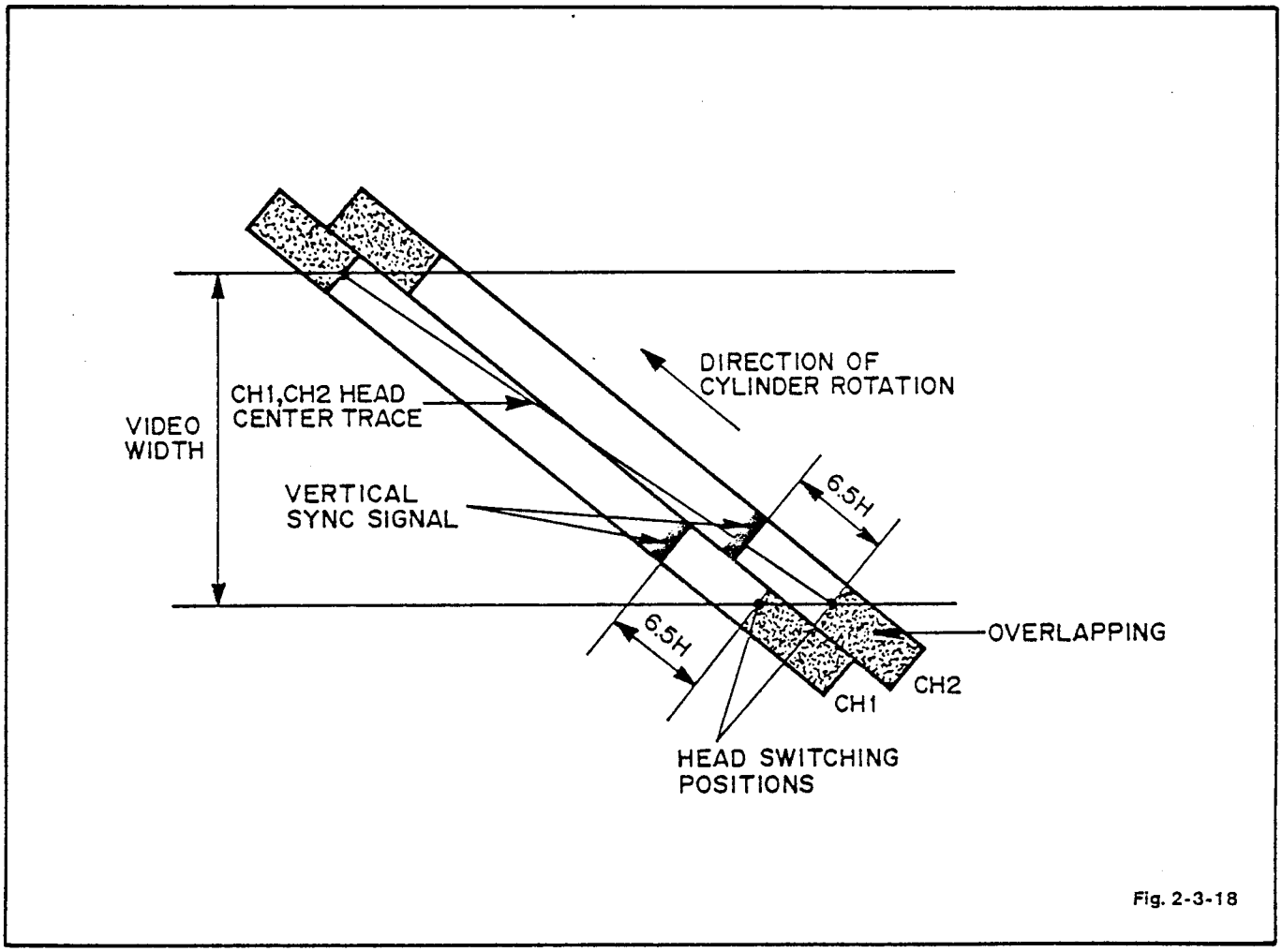


Fig. 2-3-18

At this time, the noise bar is inside the blanking period and does not appear on the TV screen.

Since the tape stops running in the playback pause mode, the playback tracing of the video head differs from that of the already recorded video track. This means in turn that the playback envelope differs from that of the normal mode, and the one shown in Fig. 2-3-19 is optimal. The playback envelope is such that as the output is reduced, the signal-to-noise ratio deteriorates and the AGC signal is output from the video circuit. It is thus sufficient if the tape stops running when synchronization is achieved between the AGC signal and the position signal at an inconspicious position off the screen.

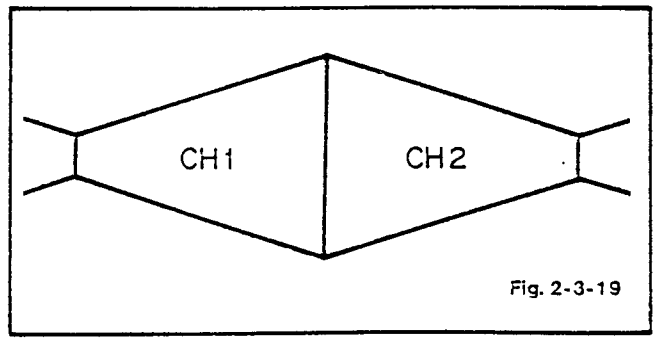


Fig. 2-3-19

Fig. 2-3-20 shows the block diagram for the STILL circit, and Fig. 2-3-21 shows the timing chart.

The capstan motor is driven by the CAP ON signal from system control in both recording and playback.

In STILL, the CAP ON signal outputs a pulse for intermittent drive for 5sec and then becomes HIGH, so that the capstan motor is stopped forcibly.

During this time, the STILL stop pulse produced by the SW 25 and the AGC pulse produced from the AGC signal are compared, the stop signal becomes HIGH when synchronization has been obtained, the capstan motor is stopped, and noise is faded out.

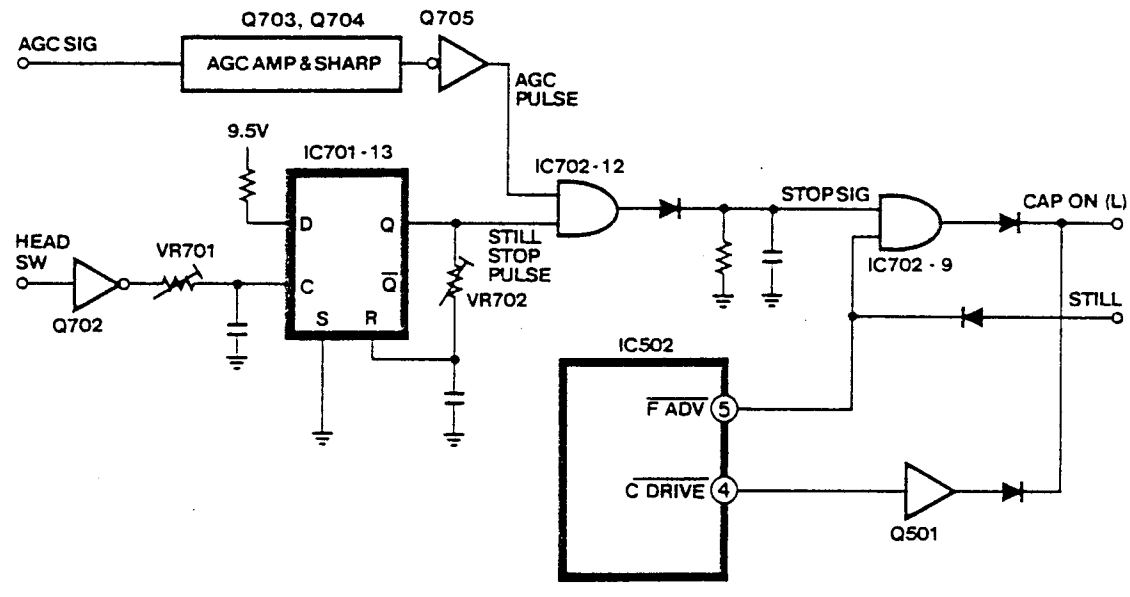


Fig. 2-3-20

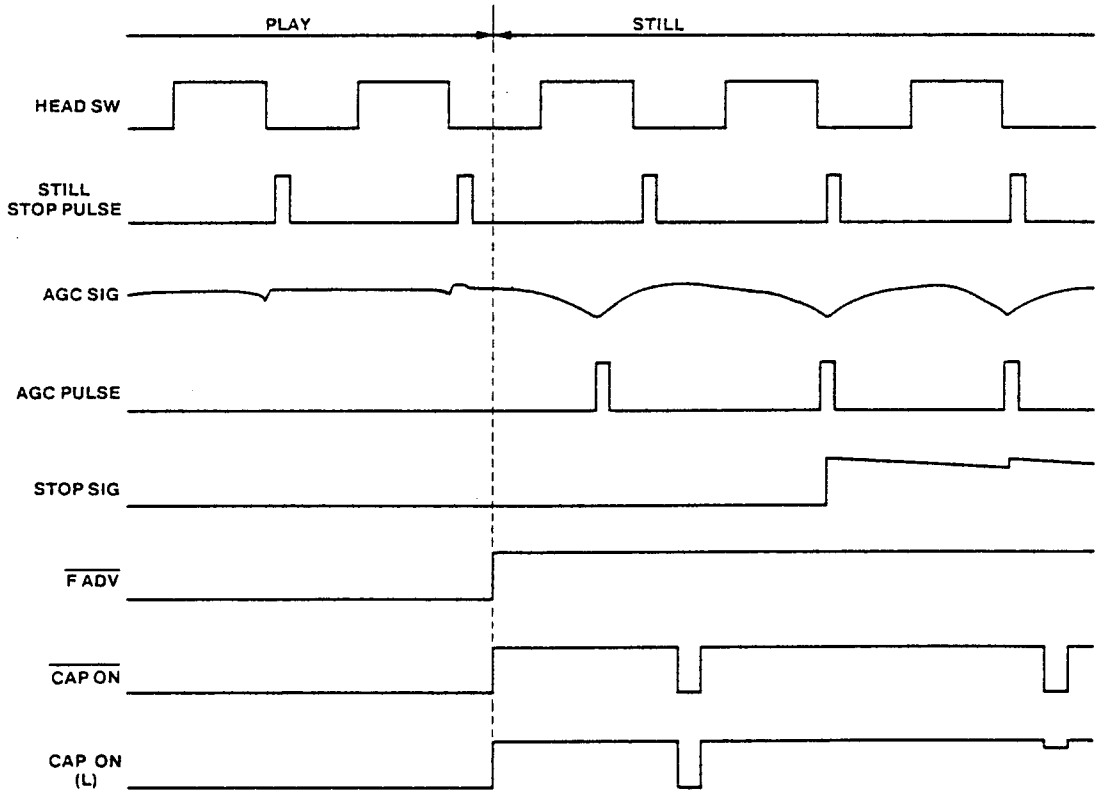


Fig. 2-3-21.

2-3-5. V-ADDITIONAL PULSE

The vertical sync signal can be disturbed during special playback (CUE, REVIEW, SLOW) by noise. To counter this, the vertical synchronization is stabilized during special playback by adding a pulse in front of the vertical sync signal, as shown in Fig. 2-3-22.

Fig. 2-3-23 shows the block diagram, and Fig. 2-3-24 shows the timing chart.

In SEARCH, MM1 and MM2 are fixed by the SEARCH (H) signal, the pulse width is decided by MM3, and the ADD VD pulse is generated.

In STILL, the flip-flop circuit of IC701 is set by the STILL (H) signal, the DIVIDED SW signal is made HIGH, and MM1 is adjusted via VR802. Next, the STILL (H) signal is passed to VR803, MM2 adjustment is executed, and the ADD VD pulse is generated in the same way as in SEARCH.

At times other than special playback, pin 2 of IC801 is made LOW, and the ADD VD output is stopped.

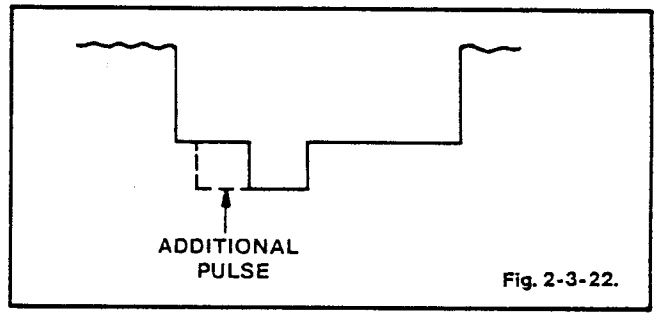


Fig. 2-3-22.

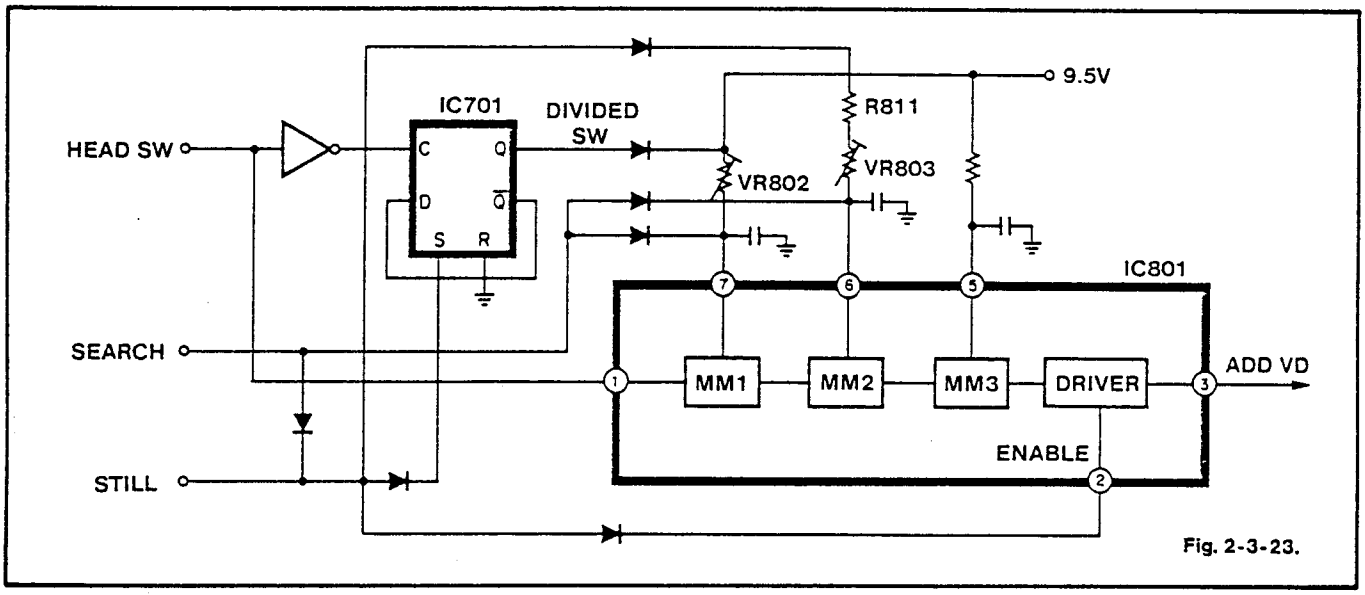


Fig. 2-3-23.

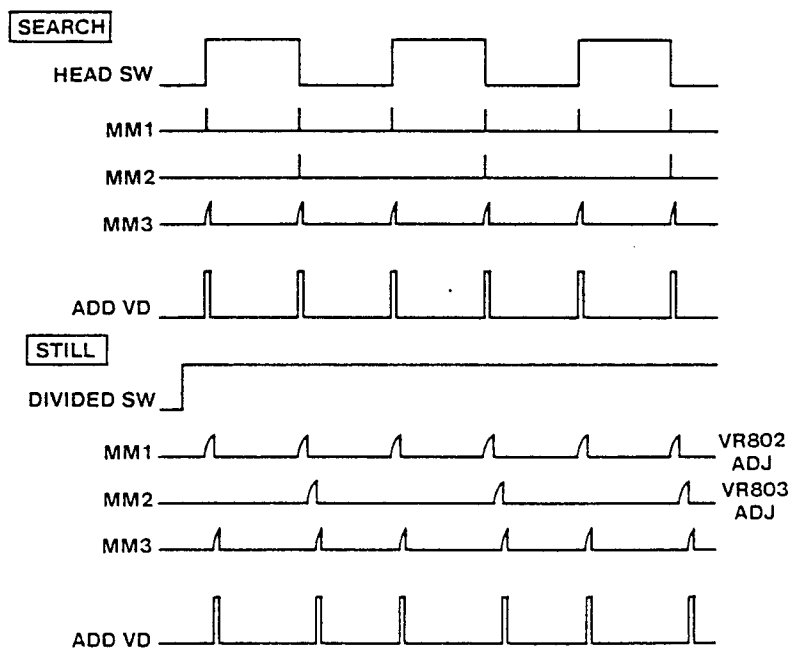
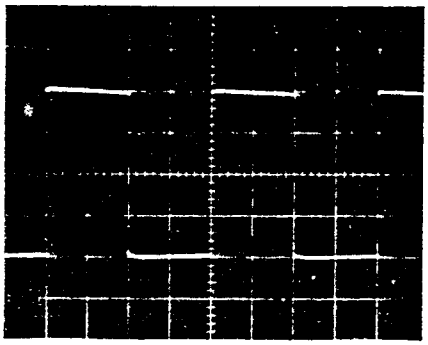


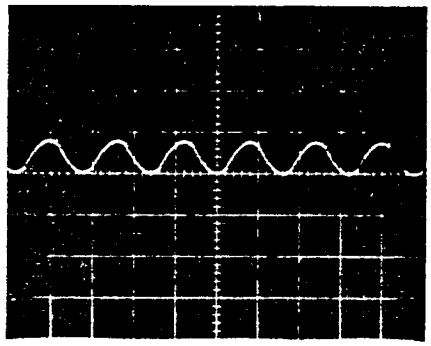
Fig. 2-3-24

2-3-6. SERVO WAVEFORMS

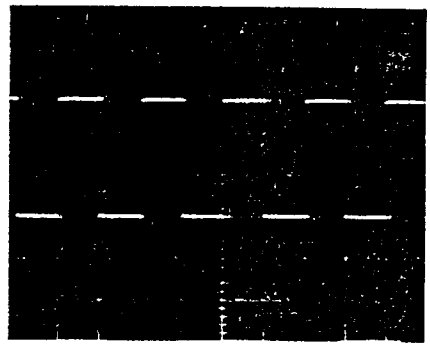
IC801 PIN 1 PB/REC
2V/10msec. div.



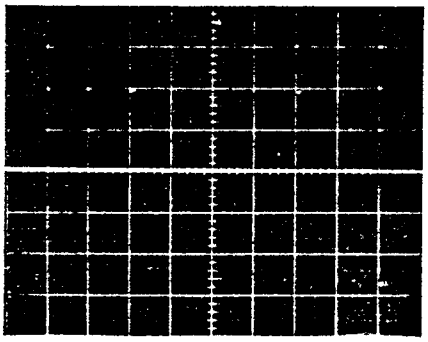
IC804 PIN 9 PB/REC
50mV/1msec. div.



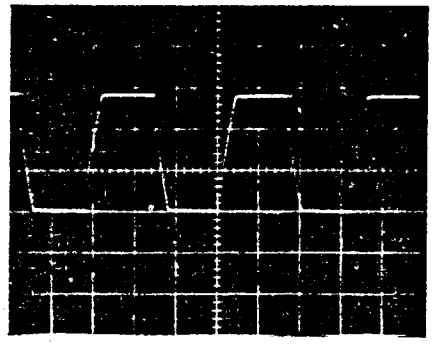
IC703 PIN 6 PB/REC
0.5V/1msec. div.



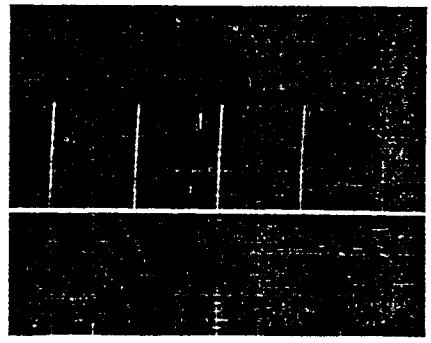
IC801 PIN 3 STILL/CUE/REV
2V/5msec. div.



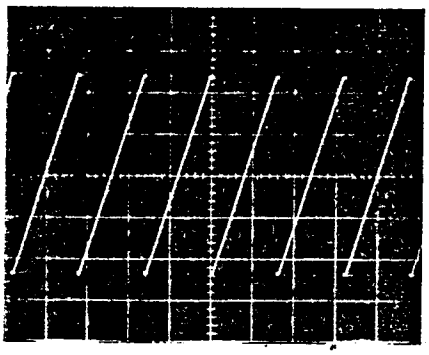
IC804 PIN 11 PB/REC
5V/0.5msec. div.



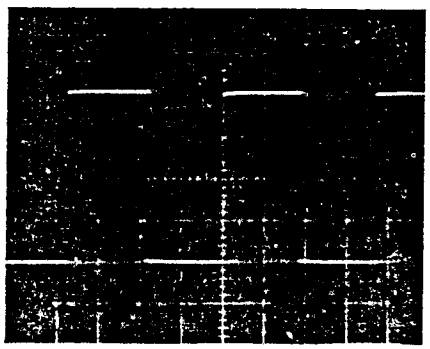
IC703 PIN 12 PB/REC
1V/20μsec. div.



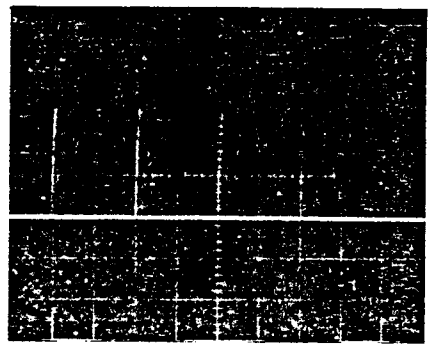
IC804 PIN 2 PB/REC
1V/1msec. div.



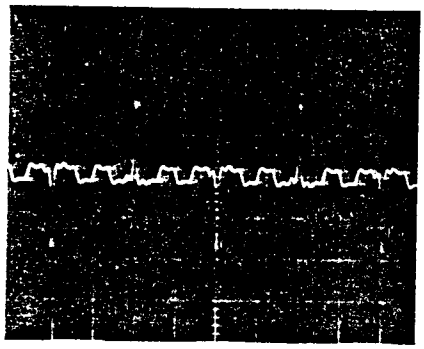
IC703 PIN 2 PB/REC
2V/0.5msec. div.



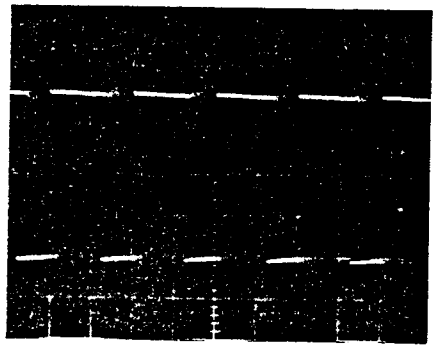
IC703 PIN 13 PB/REC
1V/20msec. div.



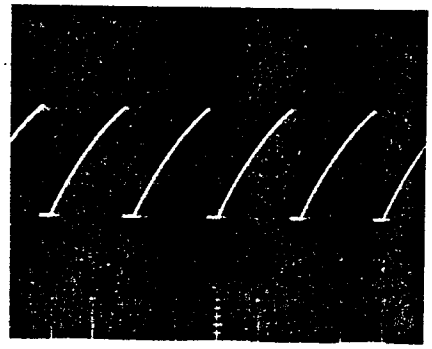
IC703 PIN 14 PB/REC
0.5V/10msec. div.



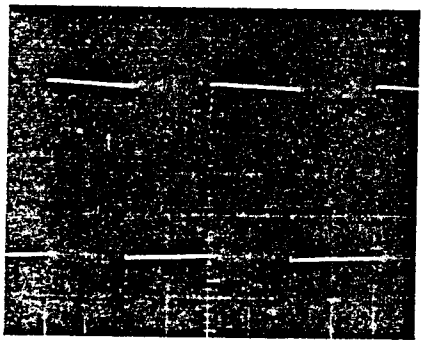
IC703 PIN 18 REC
2V/20msec. div.



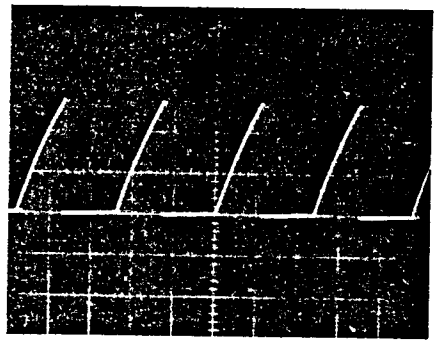
IC703 PIN 22 PB/REC
1V/20msec. div.



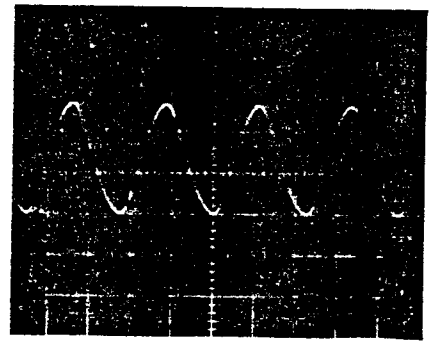
IC703 PIN 15 PB/REC
2V/10msec. div.



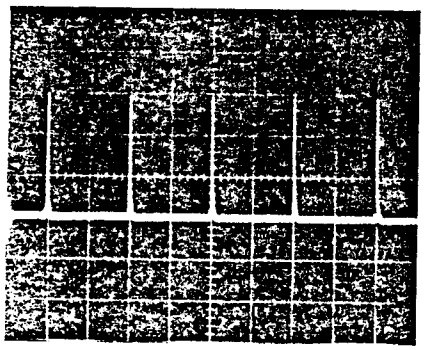
IC703 PIN 19 REC
1V/20msec. div.



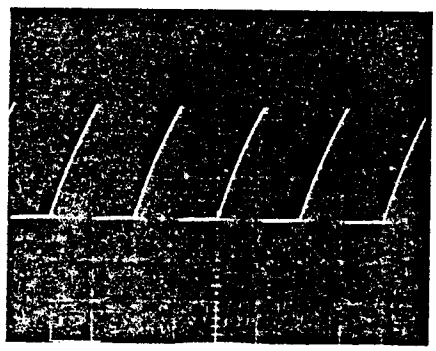
IC703 PIN 25 PB/REC
0.1V/0.1μs. div.



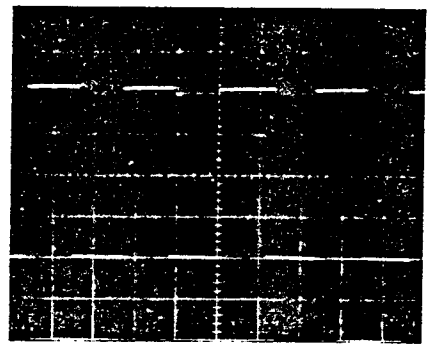
IC703 PIN 17 PB/REC
0.5V/10msec. div.



IC703 PIN 19 PB
1V/20msec. div.

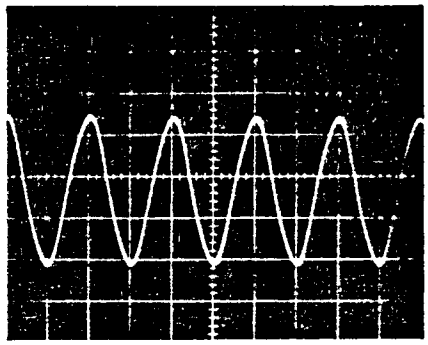


IC703 PIN 29 PB/REC
2V/0.2msec. div.

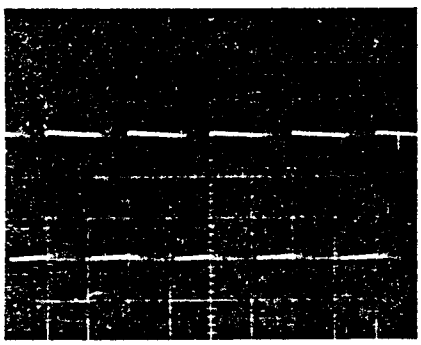


IC704 PIN 3 PB
2V/20msec. div.

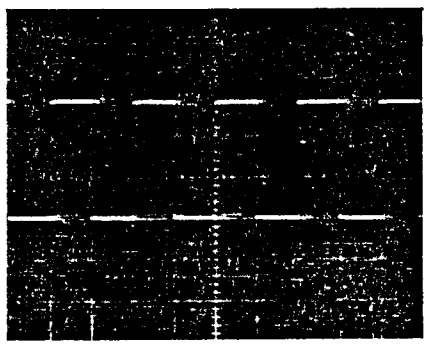
IC803 PIN 9 PB/REC
500mV/1msec. div.



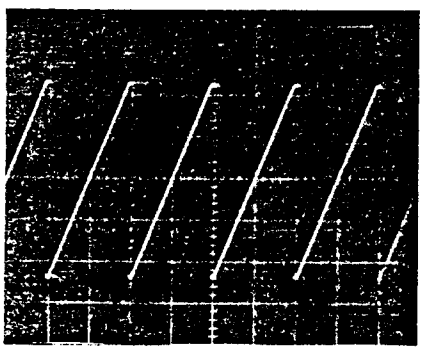
IC704 PIN 6 PB
2V/20msec. div.



IC803 PIN 11 PB/REC
0.5V/1msec. div.



IC803 PIN 2 PB/REC
1V/0.5msec. div.



2-4. AUDIO CIRCUIT

2-4-1. OUTLINE

The audio circuitry consists of an audio record/playback IC, which has various amplifiers (LINE-AMP, REC-AMP, EQUALIZER-AMP), head selector IC, 70 kHz OSC circuit, etc.

2-4-2. EE MODE

The audio input signal which is input to IC401 pin 10 is amplified by the LINE-AMP and then output from pin 12. The output signal is input to the base of Q411 via filter L403 (fH and 70 kHz trap). Q411 is an emitter follower which makes the output impedance of the signal lower. The signal is then output from the LINE OUT. (See Fig. 2-4-1)

2-4-3. PLAYBACK MODE

The audio signal picked up by the audio record/playback head is sent to IC401 pin 1. The signal, which is amplified by the playback equalizer amplifier, is output from IC401 pin 3. The signal is equalized by the time constant of NAB curve (R428, R429 and C425) so that it has a flat frequency response. After the level is adjusted by VR402, the signal is sent to IC402 pin 6 and output from pin 12 via PB amp and mute amp. The output signal is sent to the base of Q411 via the filter L403. Q411 is an emitter follower which makes the output impedance of the signal lower. The signal is then output from the LINE OUT. (See Fig. 2-4-1)

2-4-4. REC MODE

The signal path from the AUDIO IN to the LINE OUT is same as that in the EE mode. The signal is sent to IC401 pin 17 which is the input terminal of the REC-AMP after the level is adjusted by VR401 and passing through the filter L403. The amplified and high-frequency compensated signal by the REC AMP is fed through the bias trap (L401) and is superimposed on the bias signal which is output from the oscillation circuit (T401). Thus the signal is fed to the audio record/playback head and recorded on the magnetic tape. The output signal from the oscillation circuit (T401) is also supplied to the full-erase head and the audio erase head. The AGC circuit controls the input signal to avoid recording an audio signal which is above the magnetic tape saturation level. The audio signal output from the filter L403 is sent to IC401 pin 13 and is detected by the AGC circuit, by which the level of the signal, which is input to pin 10, is adjusted. (See Fig. 2-4-2)

2-4-5. Transistors Operation

Q414 An active ripple filter which is used to remove the ripple voltage from the power source.

Q413, Q412 Switching transistors which are used to supply the power source to the 70kHz oscillator during recording.

Q411 An emitter follower of the line out.

Q409 A transistor which is used to reset the AGC circuit when the EXT IN/TUNER switch is set to TUNER in case of large external signal to prevent malfunction of AGC circuit.

Q408 A transistor which is used to stop the oscillation of the 70kHz oscillator when the audio muting signal comes so that undesirable sounds during loading are not recorded on the tape.

Q407 A transistor which controls head switching IC (IC402).

Q403 A transistor which matchs the timing between audio and video signals during assemble recording by using the time constant (C411, R413 and R414).

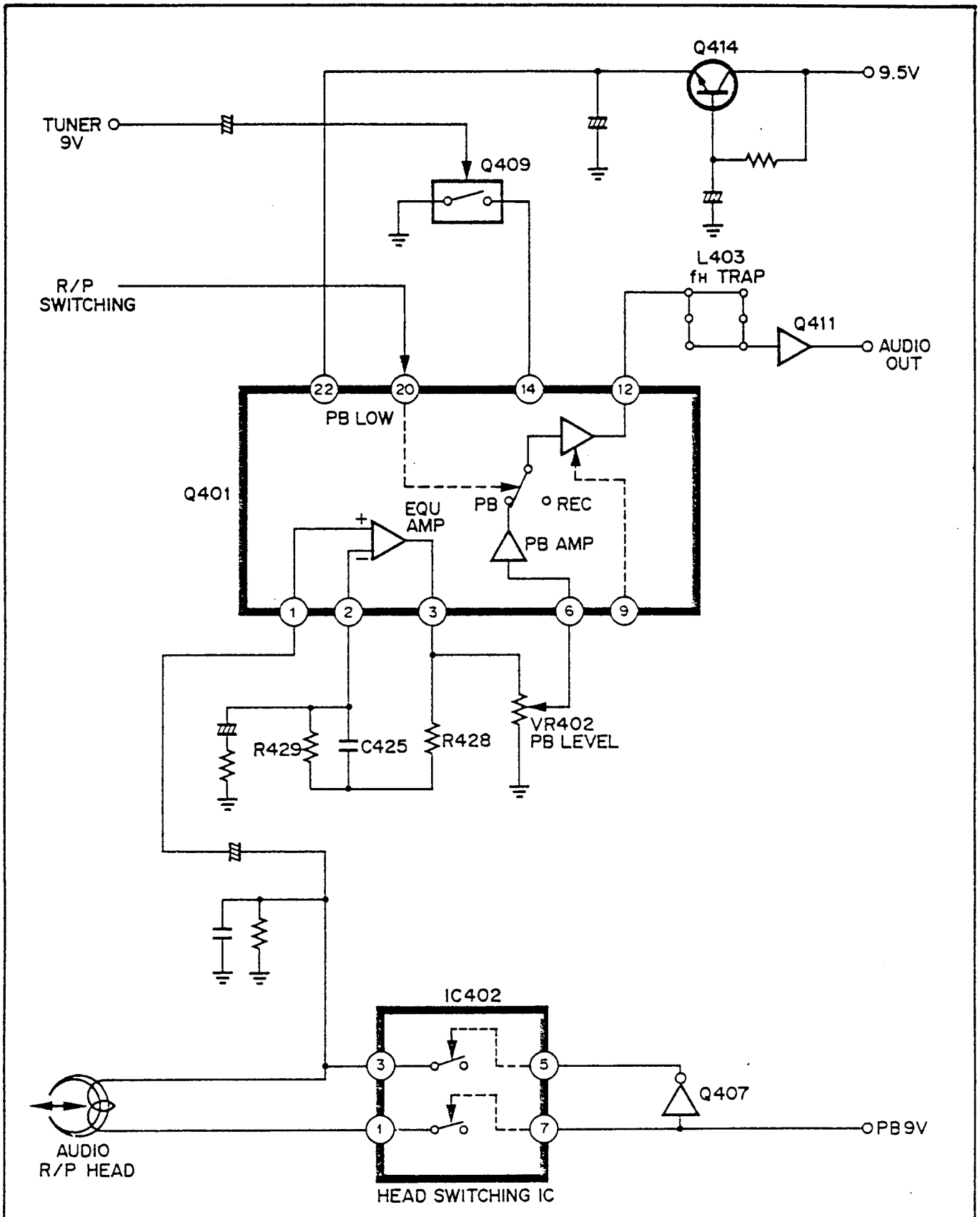

Q414
9.5V
TUNER
9V
Q409
L403
fH TRAP
R/P
SWITCHING
Q411
AUDIO
OUT
22
20
14
12
PB LOW
Q401
EQU
AMP
PB
REC
PB AMP
1
2
3
6
9
R429
C425
R428
VR402
PB LEVEL
IC402
3
5
1
7
Q407
PB 9V
AUDIO
R/P HEAD
HEAD SWITCHING IC

Fig. 2-4-1

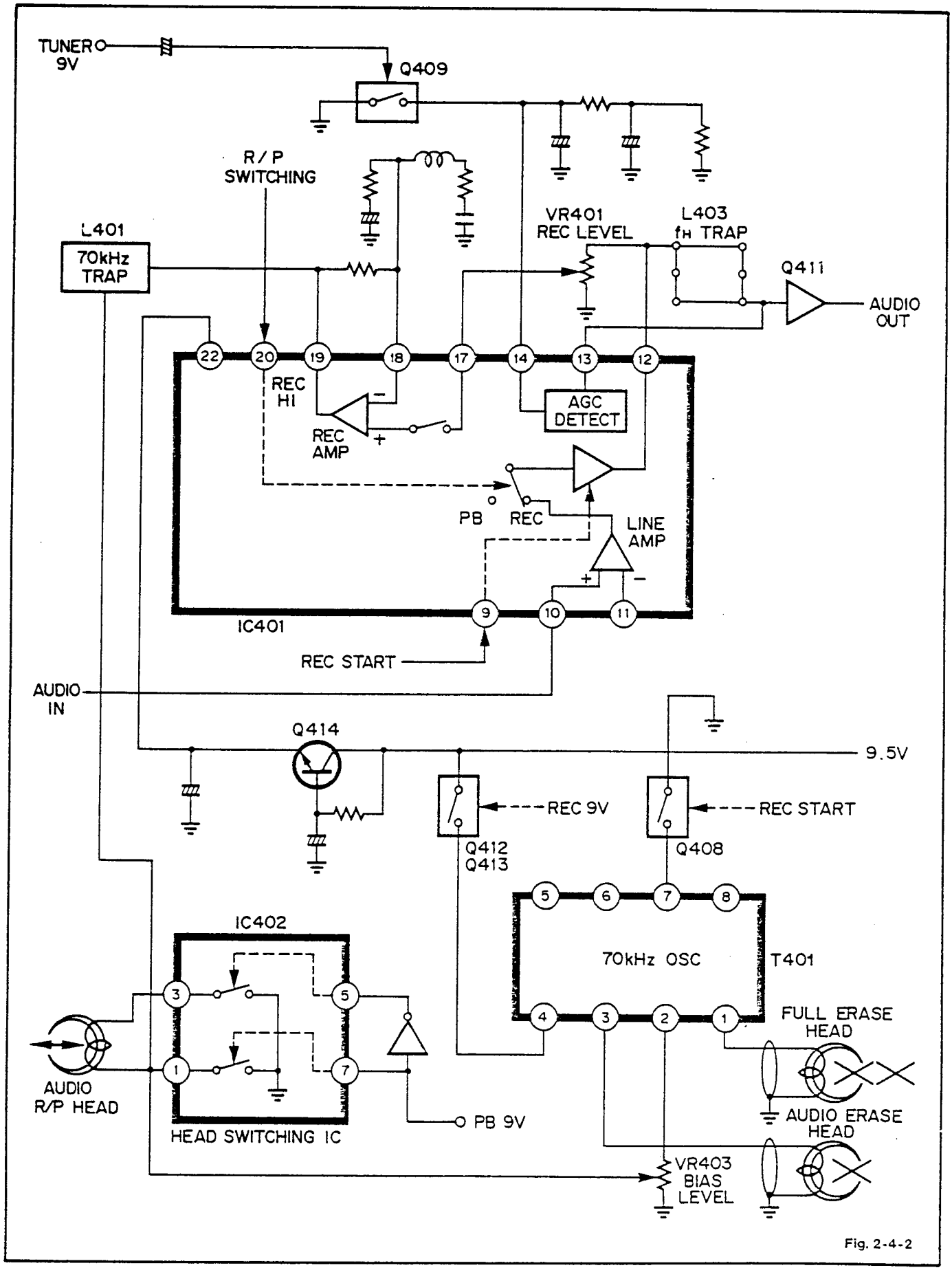

TUNER 9V
Q409
R/P SWITCHING
L401
70kHz TRAP
VR401 REC LEVEL
L403 fH TRAP
Q411
AUDIO OUT
22
20
19
18
17
14
13
12
REC HI
REC AMP
AGC DETECT
PB
REC
LINE AMP
IC401
9
10
11
REC START
AUDIO IN
Q414
9.5V
REC 9V
REC START
Q412 Q413
Q408
5
6
7
8
IC402
70kHz OSC
T401
4
3
2
1
FULL ERASE HEAD
AUDIO R/P HEAD
AUDIO ERASE HEAD
PB 9V
HEAD SWITCHING IC
VR403 BIAS LEVEL

Fig. 2-4-2

2-5. TUNER CIRCUIT

2-5-1. INTRODUCTION

The function of the tuner section is to selectively pick up off-the-air UHF TV station signals and to convert any one selected TV channel signal to a composite Video/Audio signal for use as a recording signal source for the video cassette recorder.

Fig. 2-5-1 shows the tuner block diagram identifying the main sections, which are the UHF tuner and the IF circuit board.

2-5-2. UHF TUNER SECTION

The UHF tuner has 4 varactor-tuned circuits and can be tuned to select any of the UHF TV station signals picked up by the antenna. It converts the selected UHF channel signal into an intercarrier video-sound IF signal which is processed by the video IF amplifier on the IF circuit board. The construction of the UHF tuner section is similar to tuners employed in conventional TV receivers. It has an RF amplifier, a mixer, a local oscillator and an amplifier for the video IF signal. The local oscillator is continuously and automatically fine-tuned by a control signal from the automatic fine-tuning circuit on the IF circuit board.

2-5-3. TUNER IF PCB

The IF circuit board contains all the electronic circuits required to process the intercarrier TV IF signal.

The primary functions performed by the IF circuit board are:

- Video IF amplification
- IF band pass limiting
- Linear video detection
- AGC supply for the IF amplifier
- delayed AGC supply for UHF RF amplifier
- buffered AFT signal output for UHF local oscillator correction
- sound carrier detection
- sound carrier amplification
- sound IF band pass limiting
- sound IF amplification
- AM limiting and sound detection with audio amplification

1. VIDEO IF AMPLIFIER

The intercarrier TV IF signal from the tuner IF output is fed through the IF band pass filter SF01 to IC01.

The IF signal is amplified in Q01 and appears between pins 1 and 16.

A part of the amplified video IF signal is connected to the low level detector. The 6.0MHz sound IF signal output together with the video signal is at pin 12.

2. VIDEO DETECTOR

The video signal at pins 8 and 9 of IC01 is amplified and connected to the tuned circuit T01 where it undergoes synchronous detection and then appears as the video output signal at pin 12.

3. AFT (AUTOMATIC FINE-TUNING)

The tuned circuit T02 and C18 together with the stray capacitance forms a phase shifter which causes IC01 to produce a DC output voltage at pin 5 which corresponds to any frequency deviation of the input signal (tuning error) from the video IF carrier freuency.

The AFT switch is connected to pin 6. When pins 5 and 6 are short-circuited, the AFT circuit in the IC is defeated, resulting in no output at pin 5.

4. AGC (AUTOMATIC GAIN CONTROL)

The function of the AGC circuit is to keep the output level of the detected video signal constant and independent of input signal fluctuations. The AGC signal is developed through peak level detection of the sync signal contained in the video signal. A ripple filter for both the vertical and the horizontal sync signal is connected to pin 14.

A delayed AGC voltage for automatic gain control of the UHF RF amplifiers is supplied at pin 4 through the AGC terminal of the tuner circuit as a reverse AGC voltage. The delayed RF AGC functions only with incoming antenna signals above about 70dBμ. The AGC threshold level is adjusted with VR01.

2-5-4. VIDEO AMPLIFIER

The video signal detected by IC01 is output at 1Vp-p (75Ω terminal).

The sound IF signal contained in the video signal output at IC01 is picked up by the ceramic filter F03. TR02 and TR03 are a power amplifier which delivers a current sufficient for a video signal output load with 75Ω termination.

2-5-5. SIF (SOUND IF AMPLIFIER/DETECTOR)

The detected sound IF signal at pin 12 of IC01 is connected through the 6.0MHz sound IF band pass filter F03 to the input of IC02. IC02 is a monolithic integrated circuit which contains a multi-stage IF amplifier and an amplitude limiter, and which, together with T04, 6.0MHz tuned coil filter, forms a phase discriminator.

The frequency modulated 6.0MHz sound IF signal is amplified, amplitude-limited and demodulated.

C28 connected to pin 7 completes a 75μs de-emphasis circuit.

The demodulated audio signal output is at pin 8.

2-5-6. MUTING CIRCUIT (AUDIO/VIDEO)

In the playback mode both the video and the audio signals from the tuner are muted to prevent interference with the playback signal.

The PB muting signal is a positive voltage which is applied during the playback mode only to pin 5 of terminal B. And pin 14 of IC01 is 0 volt, then at the same time, the audio muting signal is 6 volt which is applied to pin 6 of IC02.

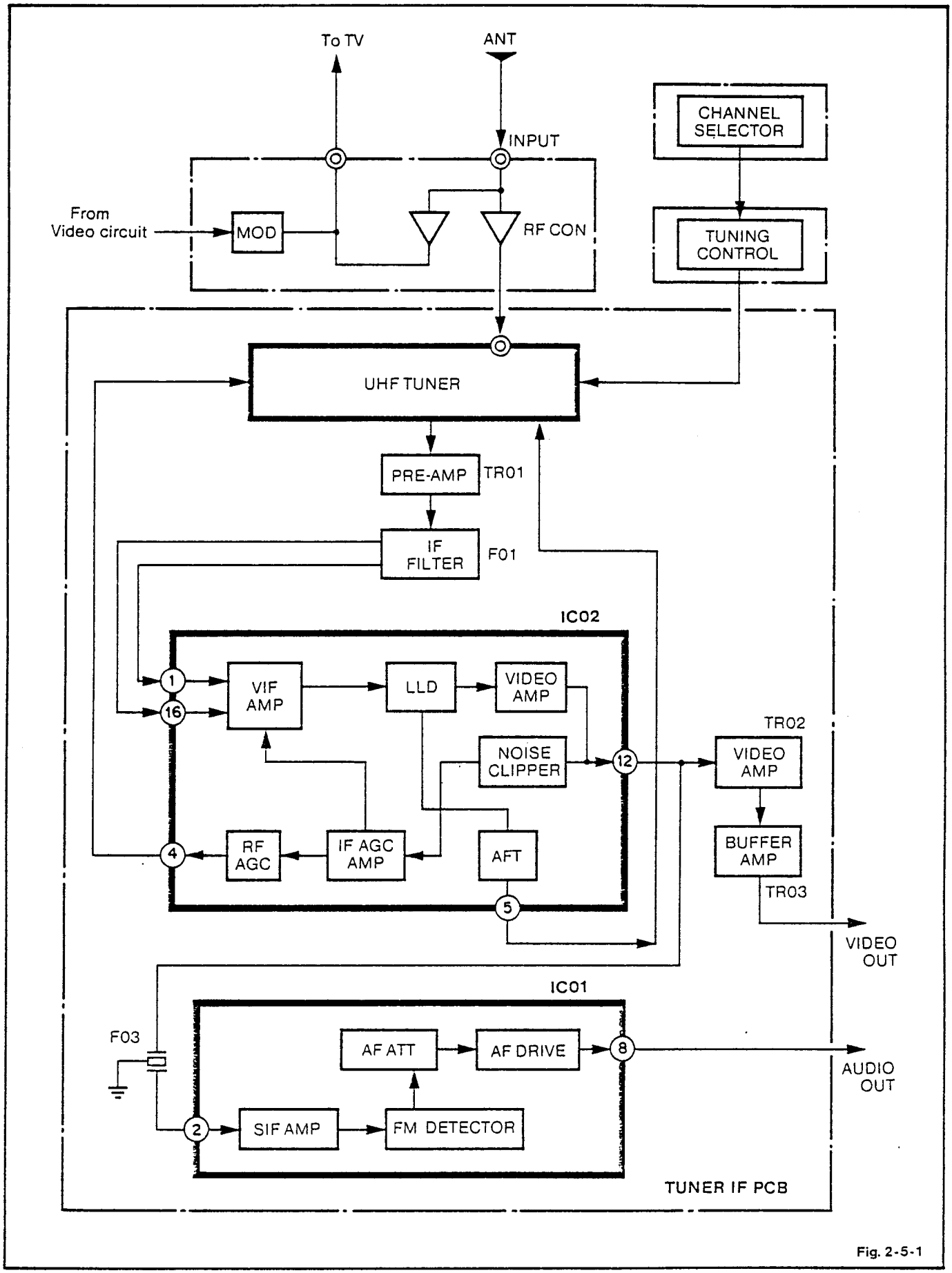

To TV
ANT
INPUT
CHANNEL SELECTOR
From Video circuit
MOD
RF CON
TUNING CONTROL
UHF TUNER
PRE-AMP
TR01
IF FILTER
F01
IC02
1
16
VIF AMP
LLD
VIDEO AMP
TR02
NOISE CLIPPER
12
VIDEO AMP
BUFFER AMP
TR03
4
RF AGC
IF AGC AMP
AFT
5
VIDEO OUT
IC01
F03
AF ATT
AF DRIVE
8
AUDIO OUT
2
SIF AMP
FM DETECTOR
TUNER IF PCB

Fig. 2-5-1

2-6. TIMER CIRCUIT

2-6-1. GENERAL

The timer circuit performs the functions of clock operation, program timer operation, tape counter operation, and memory stop operation. These functions of the timer circuit are controlled by the 4-bit microcomputer (IC101) and the electronic channel select bipolar IC (IC131).

1. CLOCK OPERATION

The AC power line frequency is used as a reference clock. The higher-frequency power line noise is removed from the signal by a low-pass filter, and after being converted into a pulse signal by the waveform shaper circuit, the signal is fed to the microcomputer. The microcomputer automatically discriminates between 50Hz and 60Hz AC line frequencies, divides the selected frequency to generate a 1-second reference pulse signal, a 1-minute signal and a 1-hour signal, for the AM/PM 12-hour display.

2. PROGRAM TIMER OPERATION

The timer is a 1-program/9-day type. When the TIMER switch is OFF and the FUNCTION switch is ON, TV program reservation can be made with the TIMER CONTROL buttons. When the TIMER SET switch is depressed, the time displayed by the clock is reset to the start time of the program being reserved. When the pre-set time is reached, the record signal (HIGH) is sent to the system control circuit and recording of the program commences.

3. TAPE COUNTER OPERATION

The tape counter is an electronic counter which indicates the current position of the tape. The rotation of the take-up reel is counted. The count direction [UP (HIGH), DOWN (LOW)] is determined by the F/R signal from the system control circuit, and this provides a 4-digit signal which represents the current position of the tape.

4. MEMORY STOP OPERATION

The tape can be automatically rewound to the position where the tape counter was cleared (reset to 0000). If the COUNTER MEMORY button has been pushed and the display set to MEMORY, when the tape counter changes from 0000 to 9999, the stop signal (HIGH) is sent to the system control and the rewind operation stops.

2-6-2. CIRCUIT OPERATIONS

Fig. 2-6-1 shows a block diagram for Timer Circuit operation.

1. BASIC OPERATION OF THE TIMER MICROCOMPUTER (IC101)

Table 2-6-1 shows the functions of the input/output ports of the microcomputer. IC101 is driven by two basic pulses. The operation of the microcomputer will stop immediately when either one of the pulses stops. One pulse is the 500 kHz pulse from the ceramic resonator (CR101), and the other is the 50 Hz pulse obtained from the AC power supply via Q1001.
The 500 kHz pulse is a slightly distorted sine wave with an amplitude of 5 Vp-p. This pulse governs the basic operation of the microcomputer, and when it stops, all timer functions stop.
The 50 Hz pulse has an amplitude of about 90 Vp-p at pin 1 of PV113. It passes through the low pass filter R1029 to R1031, R1039, C1004, and C1008. It appears as a 5 Vp-p square wave at the collector of Q1001, and is applied to port A0 of the microcomputer. This 50 Hz pulse governs the progress of the clock.

2. KEY MATRIX

The 4 x 4 = 16 key matrix is composed of the four input ports (B0 to B3) and the four output ports (H0 to H3) of the microcomputer driving the segments of the Digitron (fluorescent tube). Table 2-6-2 shows the key matrix allotment. Actually, 12 input signals are taken in, and D1001 to D1014 and Q1003 to Q1005 are the parts of which the matrix is composed. The signals taken in from the key matrix include the cassette status and the FUNCTION switch ON/OFF status in addition to the signals from the operation buttons.
The key scanning speed is about 83 Hz.
In addition to the cassette and power status signals read in from the key matrix, the VCR operation mode signals PAUSE, PB, REC, and TIMER SET are read in from the input ports D0 to D3 of the microcomputer. Timer REC output (port C1), memory stop output (port C2), timer LED ON/OFF output (port C3), and channel selection control (port C0 and I1) are also executed.

3. DIGITRON OPERATION

The eight segment and the nine grid terminals are pulled down to − 20 V via the block resistors BR101 and R1007, R1020 ~ R1024. The filament is pulled down to − 20 V via power transformer winding and ZD101. The display brightness is set by these − 20 V levels and ZD101. Grid and segments are driven by IC101 as shown in table 2-6-3.

4. POWER SUPPLY

Independent of the ON/OFF position of the FUNCTION switch, the voltages shown in tables 2-6-4 (A) and 2-6-4 (B) are supplied to the timer circuit via the connectors PV104, PV105 and PV109 when the power cord is plugged into an AC wall outlet.
Pin 1 of PV103 and pin 2 of PV004 supply power to the tape counter (reel sensor) and the tuner circuit respectively.

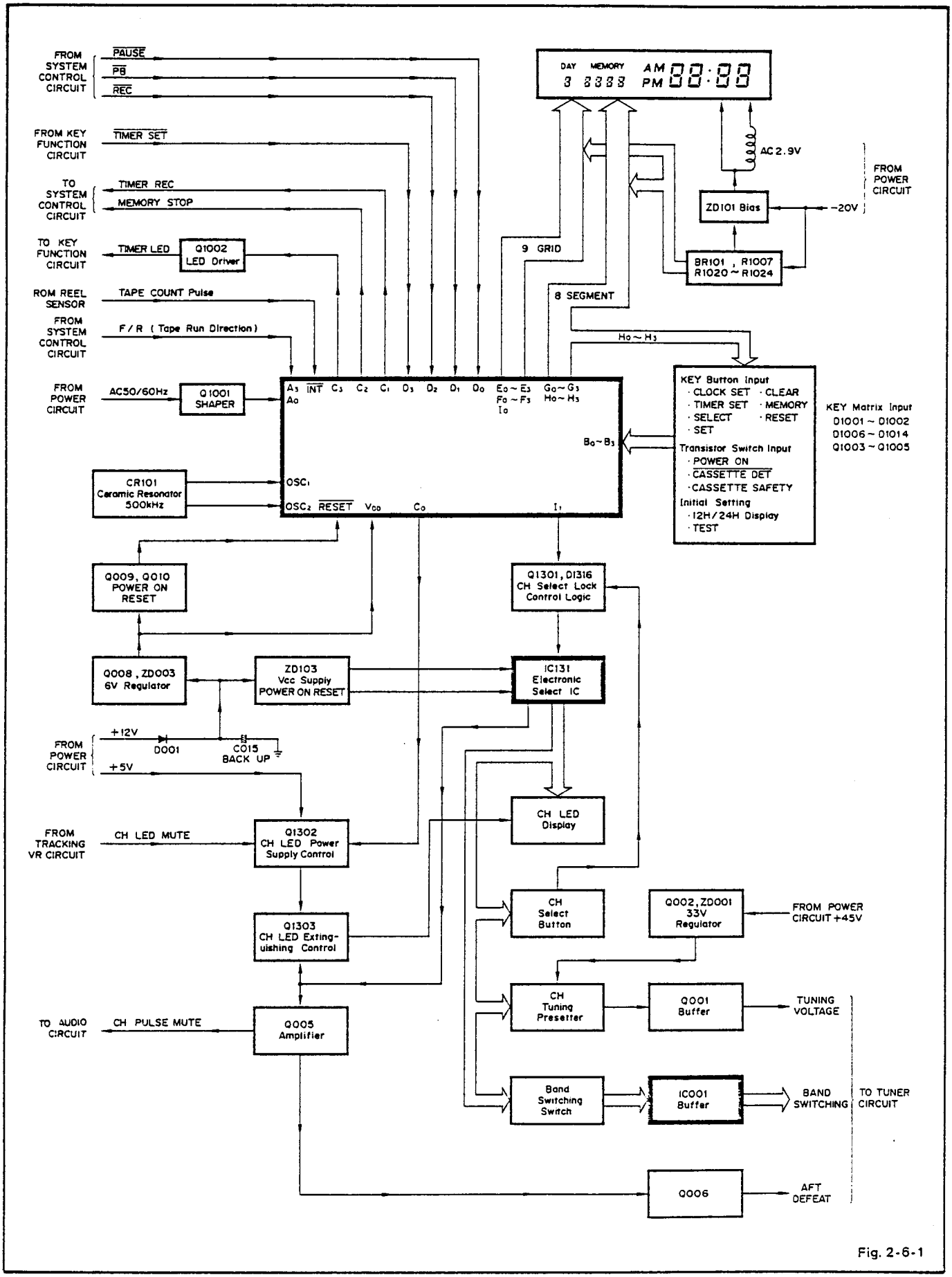

FROM SYSTEM CONTROL CIRCUIT
PAUSE
PB
REC
FROM KEY FUNCTION CIRCUIT
TIMER SET
TO SYSTEM CONTROL CIRCUIT
TIMER REC
MEMORY STOP
TO KEY FUNCTION CIRCUIT
TIMER LED
Q1002 LED Driver
ROM REEL SENSOR
TAPE COUNT Pulse
FROM SYSTEM CONTROL CIRCUIT
F / R (Tape Run Direction)
FROM POWER CIRCUIT
AC50/60Hz
Q1001 SHAPER
DAY MEMORY AM PM 88:88
AC 2.9V
FROM POWER CIRCUIT
ZD101 Bias
-20V
9 GRID
8 SEGMENT
BR101 , R1007 R1020 ~ R1024
H0 ~ H3
KEY Button Input
· CLOCK SET · CLEAR
· TIMER SET · MEMORY
· SELECT · RESET
· SET
Transistor Switch Input
· POWER ON
· CASSETTE DET
· CASSETTE SAFETY
Initial Setting
· 12H/24H Display
· TEST
KEY Matrix Input
D1001 ~ D1002
D1006 ~ D1014
Q1003 ~ Q1005
A3 INT C3 C2 C1 D3 D2 D1 D0 E0 ~ E3 G0 ~ G3
A0 F0 ~ F3 H0 ~ H3
I0
B0 ~ B3
OSC1
OSC2 RESET VDD C0 I1
CR101 Ceramic Resonator 500kHz
Q009, Q010 POWER ON RESET
Q1301, D1316 CH Select Lock Control Logic
Q008 , ZD003 6V Regulator
ZD103 Vcc Supply POWER ON RESET
IC131 Electronic Select IC
FROM POWER CIRCUIT
+12V
D001
C015 BACK UP
+5V
CH LED Display
FROM TRACKING VR CIRCUIT
CH LED MUTE
Q1302 CH LED Power Supply Control
CH Select Button
Q002, ZD001 33V Regulator
FROM POWER CIRCUIT +45V
Q1303 CH LED Exting-uishing Control
CH Tuning Presetter
Q001 Buffer
TUNING VOLTAGE
TO AUDIO CIRCUIT
CH PULSE MUTE
Q005 Amplifier
Band Switching Switch
IC001 Buffer
BAND SWITCHING
TO TUNER CIRCUIT
Q006
AFT DEFEAT

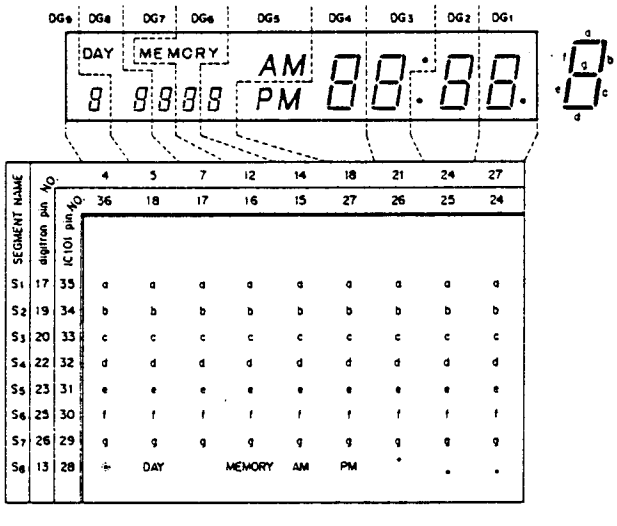
Fig. 2-6-1

PIN	I/O	Active level	Port	FUNCTION
2	I	High	A_3	Tape run direction input (high when tape is running in forward direction)
3	I		B_0	Key scan input
4	I		B_1	Key scan input
5	I		B_2	Key scan input
6	I		B_3	Key scan input
7	O	Low	C_0	CHANNEL LED power supply control
8	O	High	C_1	TIMER REC output
9	O	High	C_2	MEMORY STOP output
10	O	Low	C_3	TIMER LED drive
11	I	Low	D_0	TIMER SET input
12	I	Low	D_1	PB input
13	I	Low	D_2	REC input
14	I	Low	D_3	TIMER SET input
15	O		E_0	Digitron grid drive
16	O		E_1	Digitron grid drive
17	O		E_2	Digitron grid drive
18	O		E_3	Digitron grid drive
19	I	Low	RES	POWER ON RESET input
21			V_{SS}	Ground
22	I		OSC_1	Clock oscillation frequency setting input
23	O		OSC_2	Clock oscillation frequency setting input
24	O		F_0	Digitron grid drive
25	O		F_1	Digitron grid drive
26	O		F_2	Digitron grid drive
27	O		F_3	Digitron grid drive
28	O		G_0	Digitron segment drive
29	O		G_1	Digitron segment drive
30	O		G_2	Digitron segment drive
31	O		G_3	Digitron segment drive
32	O		H_0	Digitron segment drive, key scan output
33	O		H_1	Digitron segment drive, key scan output
34	O		H_2	Digitron segment drive, key scan output
35	O		H_3	Digitron segment drive, key scan output
36	O		I_0	Digitron grid drive
37	O	Low	I_1	Channel lock control (low at the time of channel lock)
38	I	Low	HOLD	Connected to V_{DD} (microcomputer stops when this becomes low)
39	I	Low	INT	TAPE COUNT pulse input
40	I		V_{DD}	Power supply
41	I		A_0	AC 50/60 Hz clock pulse input

Table 2-6-1

IC101 PORT	B3	B2	B1	B0
H0	TEST	12H/24H DISPLAY		
H1	TIMER SET KEY	CLOCK SET KEY	RESET KEY	MEMORY KEY
H2		CLEAR KEY	SET KEY	SELECT KEY
H3		CASSETTE SAFETY	CASSETTE DETECTOR	POWER ON

Table 2-6-2



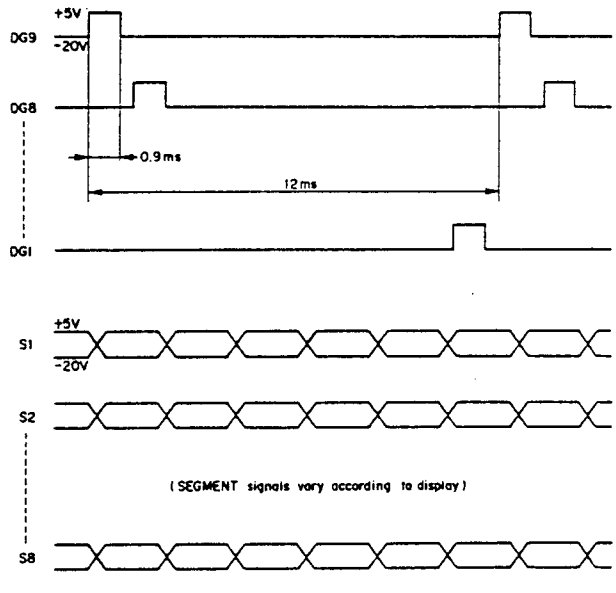


Table 2-6-3

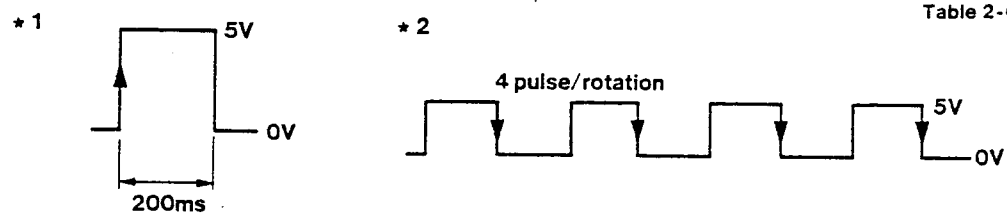
NOTE:
The position marked * is for TV/VCR selection.
When VCR is selected, S_8 goes HIGH when DG_9 is high, and TV is selected, S_8 never goes HIGH when DG_9 is HIGH.
Example for Flourescent Display operaton: "Second" dot flashing operation.
The dot is lit when both S_8 and DG_1 are HIGH and goes out when S_8 becomes LOW even if DG_1 is HIGH.

Connector	Pin	I/O	Pin name	Signal level	
PV109	1		GND		
	2		+12V		
	3	I	RESET	ON : 1V	OFF : 5V
	4		BACK UP +12V		
	5		BACK UP +5V		
PV106	1	I	+9.5V	ON : 9.5V	OFF : 0V
	2	I	PAUSE OUT	ON : 1V	OFF : 9.5V
	3	I	PB OUT	ON : 1V	OFF : 9.5V
	4	I	REC OUT	ON : 1V	OFF : 9.5V
	5	I	CDT SIG	Cassette presence : 0V	No cassette : 5V
	6	O	TIMER REC	ON : 5V	OFF : 0V
	7	I	SAFETY	Tab presence : 5V	No tab : 0V
	8		GND		
PV104	1	I	AC 2.9V	$5.8V_{p\text{-}p}$	
	2		NC		
	3	I	AC 2.9V	$5.8V_{p\text{-}p}$	
PV105	1		+12V		
	2		NC		
	3		−20V		
	4		GND		
PV101	1	O	COUNTER STOP	* 1	
	2	O	TAKE UP PULSE	* 2	
	3	I	F/R	Forward : 5V	Reverse : 0V
	4		GND		
PV103	1		+12V		
	2		GND		
	3	I	TAKE UP PULSE	* 2	
PV108	1		NC		
	2	I	TIMER SET	ON : 0V	OFF : 5V
	3		GND		
PV114	1		NC		
	2	O	TIMER LED	ON : 0V	OFF : 5V
PV112	1	O	LED CONTROL	ON : 5V	OFF : 0V
	2		+5V		

Table 2-6-4 (A)

Connector	Pin	I/O	Pin name	Signal level
PV113	1	I	50/60Hz	90Vp-p
	2		+5V	
PV107	1		+12V	
	2		GND	
PV110	1	O	CH 1	33V or 0V (Selected)
	2	O	CH 2	33V or 0V (Selected)
	3	O	CH 3	33V or 0V (Selected)
	4	O	CH 4	33V or 0V (Selected)
	5	O	CH 5	33V or 0V (Selected)
	6	O	CH 6	33V or 0V (Selected)
	7		GND	
	8	O	AFT DEF	5V or 0V (Changed)
PV111	1	O	CH 7	33V or 0V (Selected)
	2	O	CH 8	33V or 0V (Selected)
	3	O	CH 9	33V or 0V (Selected)
	4	O	CH 10	33V or 0V (Selected)
	5	O	CH 11	33V or 0V (Selected)
	6	O	CH 12	33V or 0V (Selected)

Table 2-6-4 (B)



5. POWER-ON RESET FOR THE TIMER MICROCOMPUTER

When the AC power is ON, the reset pulse shown in Fig. 2-6-2 is sent to pin 19 of the microcomputer (IC101), and the microcomputer is reset.
The timing for generating the reset pulse (active low) is decided by the voltage drop in forward direction of the LED (D002) and the voltage drop in forward direction between the base and the emitter of Q009. When the power supply voltage rises to about 80% of the normal value of VDD 5.6 V, a positive pulse is applied to pin 19 via Q010. At the time of normal operation, the value is fixed to + 5.6 V.

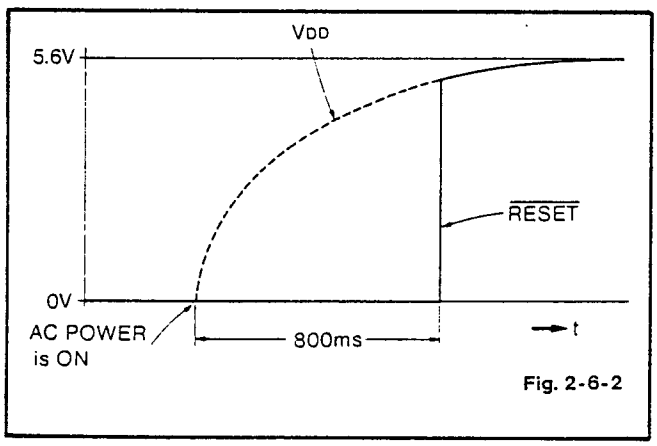


Fig. 2-6-2

6. POWER-ON RESET FOR THE ELECTRONIC CHANNEL SELECT IC (IC131)

In the same way as for the timer microcomputer, POWER-ON reset is also required for this IC. When resetting is incomplete, the CH LED may not light up. When the DC power supply voltage rises to about 65% of the normal value (12 V) when the AC power is ON, the reset voltage is applied via ZD103, and the initial CH position always keeps to the preset #1 position.

7. MOMENTARY POWER FAILURE BACK-UP FUNCTION

In case a momentary power failure of less than 1.0 sec occurs, the reserved timer program, the present time, and the selected CH position will not be lost.

- Back-up operation for the timer microcomputer (IC101):
  In the case of a momentary power failure, D001 opens, and the charge stored in C015 is used to continue the operation of IC101.

- Back-up operation for the electronic channel select IC (IC131):
  The selected channel position of IC131 is held by D001 and C015 in the same way as described above.

8. CHANNEL SELECT PROHIBITION CONTROL

To lock the selected channel position during REC, PLAYBACK, etc., a low signal from port I1 of the microcomputer is transmitted to Q1301 to cut off this transistor, and even when the channel select buttons S1301 to S1312 are depressed, no voltage is supplied to pin 18 of IC131, so that the selected channel position is locked.

9. ELECTRONIC CHANNEL SELECT OPERATION

Fig. 2-6-3 is a rough wiring diagram for the electronic channel select operation.

When no channel is selected (no CH LED is lit), the ports K1 to K16 all are open (= OFF).

When, for example, the button S1301 is depressed, voltage is fed to pin 18 via R1301, immediately after the port K1 is short-circuited to ground and locked. The LED D1301 lights, and PRESET #1 is selected. The tuning voltage is supplied to the tuner circuit via D031 and Q001.

The 2 kHz oscillator circuit formed of R1302 and C1303 oscillates only during the transition period from depressing the channel select button until this channel has been tuned.

10. CH LED POWER SUPPLY CONTROL

To extinguish the CH LED during PLAYBACK, TIMER REC stand-by, etc., a high signal is transmitted from the port C0 of the microcomputer to Q1302, this transistor is cut off, and the power supply to the CH LED is interrupted.
Even when the TUNER/EXT IN switch on the front panel is set to "EXT IN", Q1302 will be cut off and the CH LED will be extinguished.

11. AFT DEFEAT AND CH PULSE MUTE

The AFT defeat pulse (negative) is output from pin 13 of IC131 only during the transition period of the CH select operation. After polarity change and waveform shaping by Q005, it is divided into three routes.

1) It is supplied as it is to the audio circuit to mute the noise during CH switching.
2) It is fed to the CH LED extinguishing control Q1303 to prevent momentary lighting of all CH LEDs during the CH switching transition period.
3) It is fed to the tuner circuit as the AFT defeat pulse via Q006.

12. TUNING VOLTAGE REGULATOR

The + 45 VDC supplied from the power supply is reduced to + 33 VDC, stabilized by Q003, Q002 and ZD001 and supplied to the tuning preset VR.

13. TAPE COUNTER OPERATION

The tape counter executes count up or down for the revolutions of the take-up reel shaft. (It does not indicate the actual tape run amount.)
8 pulses per revolution are applied to pin 39 of the microcomputer via the system control servo circuit. Only the negative going edge is read and counted, and 1 count per 4 pulses, i.e. 2 counts/revolution, is counted up or down.
The count direction (up or down) is dependent on the F/R signal (pin 3 of PV101) from the system control circuit. When this signal is high, a count-up instruction is given to A3 of the microcomputer, and when this signal is low, a count-down instruction is given to A3.

14. MEMORY STOP (OR COUNTER STOP) OPERATION

When the count value during rewinding in the MEMORY mode changes from 0000 to 9999, a pulse (active high) of 200 ms is output from port C2 of the microcomputer and supplied to the system control circuit.

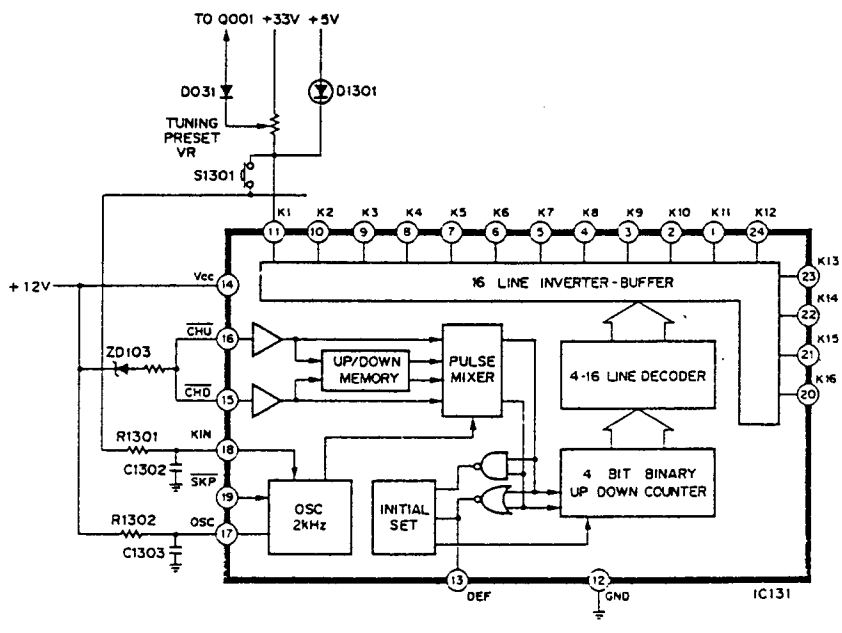


Fig. 2-6-3

2-7. POWER SUPPLY CIRCUIT

2-7-1. GENERAL

The power supply circuit employs a power transformer; the secondary side consists of a series control type regulated power supply using a hybrid IC which controls the output voltage. (Fig. 2-7-1 shows block diagram and Fig. 2-7-2 shows IC interior equivalent circuit.)

2-7-2. PRIMARY SIDE

This consists of the POWER A PCB. C901 is a line shunt capacitor which prevents high harmonic components generated within the set from leaking outside through the power supply cord.

2-7-3. SECONDARY SIDE

This consists of the POWER A, POWER B and POWER C PCB.

1. 19.5V RECTIFICATION CIRCUIT

The AC power supplied from the POWER A PCB is bridge rectified by D905 ~ D908 and smoothed by C912. The 19.5V DC is fed into the hybrid IC (IC901, STK5322HSL), which has two regulated power supply circuit, and is used as the dew prevention heater power supply for cylinder.

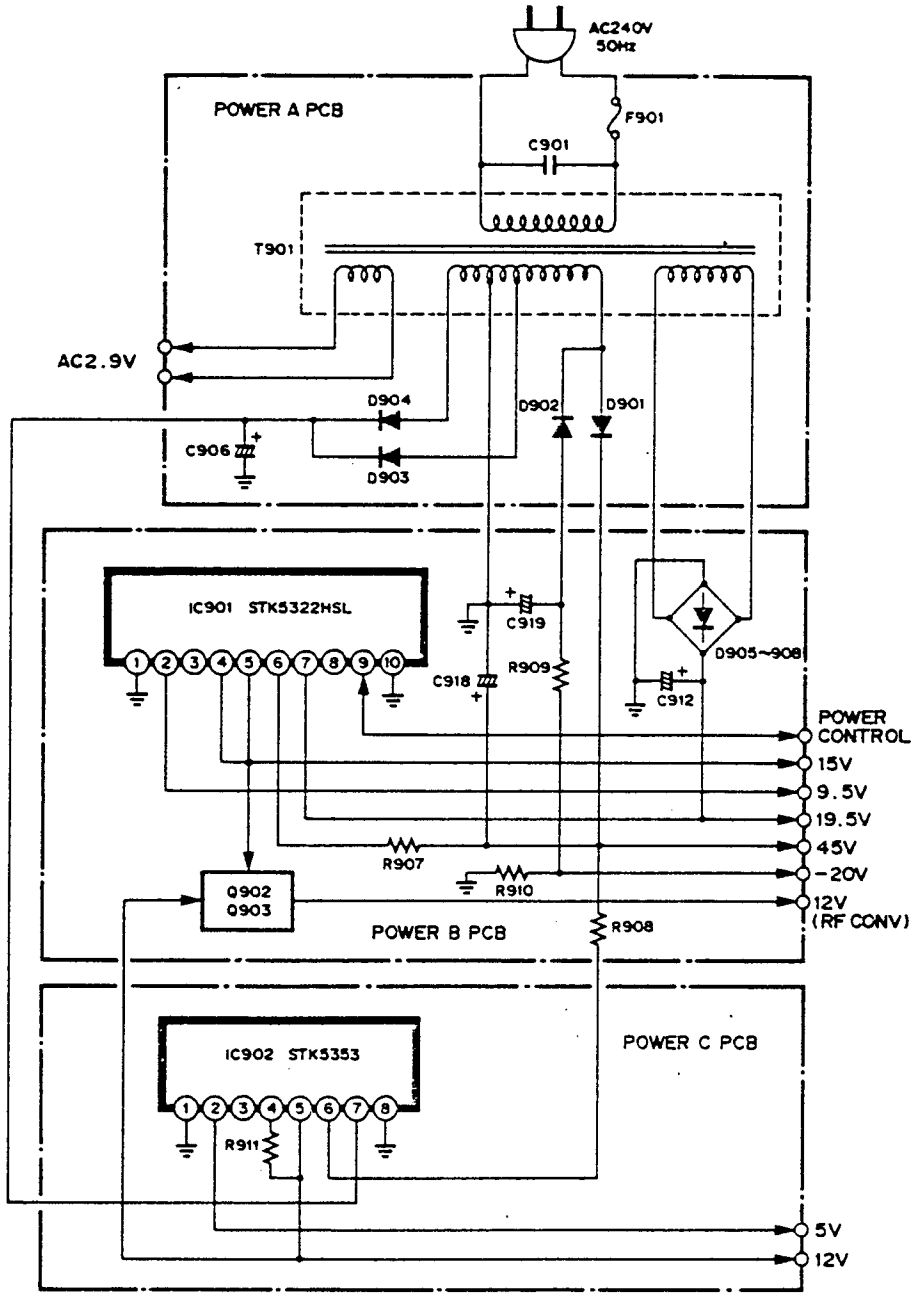


Fig. 2-7-1

2. 15V REGULATED POWER SUPPLY CIRCUIT

The 19.5V DC is applied to IC901 pin 7 of POWER B PCB and a more regulated 15V DC is obtained from IC901 pin 5. This 15V DC is fed into the system control circuit as the servo circuit operation power supply and is also used as the 9.5V DC regulated power supply. This circuit is controlled by the power control signal from IC901 pin 9. When the POWER switch in "ON", the control signal is set to "LOW" and 15V DC is output.

3. 9.5V REGULATED POWER SUPPLY CIRCUIT

The 15V DC output from IC901 pin 5 is fed to IC901 pin 4 and 9.5V DC is obtained from IC901 pin 2. This regulated power supply is sent to system control circuit and is also used as a PB9V and REC 9V for video circuit, etc.

4. 12V REGULATED POWER SUPPLY CIRCUIT

The 16V DC obtained from full-wave rectifier (D903, D904) and smoothing circuit (C906) inside POWER A PCB is applied to IC902 (STK5353) pin 7 which has 2 regulated power supply circuit, and a regulated 12V DC is obtained from IC902 pin 5. This voltage is used as the TUNER/IF unit and RF converter power supply and is also used as 5V DC power supply.
The power supply for RF converter is controlled by the POWER switch via Q902, Q903 and 15V regulated power supply.

5. 5V REGULATED POWER SUPPLY CIRCUIT

The 12V DC is applied to IC902 pin 4 on POWER C PCB via fuse resistor R911 and regulated 5V DC is obtained from IC902 pin 2. This voltage is always supplied to the system control and timer circuits independent of the function switch position.

6. 45V REGULATED POWER SUPPLY CIRCUIT

The power supply is half-wave rectified by D901 and smoothed by C918 and 45V is obtained. This voltage is used as the tuning voltage for presetter circuit and is also used as bias voltage for IC901 and IC902 via R907 and R908.

7. −20V REGULATED POWER SUPPLY CIRCUIT

The power supply is negative side half-wave rectified by D902 and smoothed by C919. The −20V DC is obtained by divided with R909 and R910.
This voltage is used as the grid voltage for FL tube.

8. AC 2.9V

This is the power supply for the FL tube heater of timer circuit.

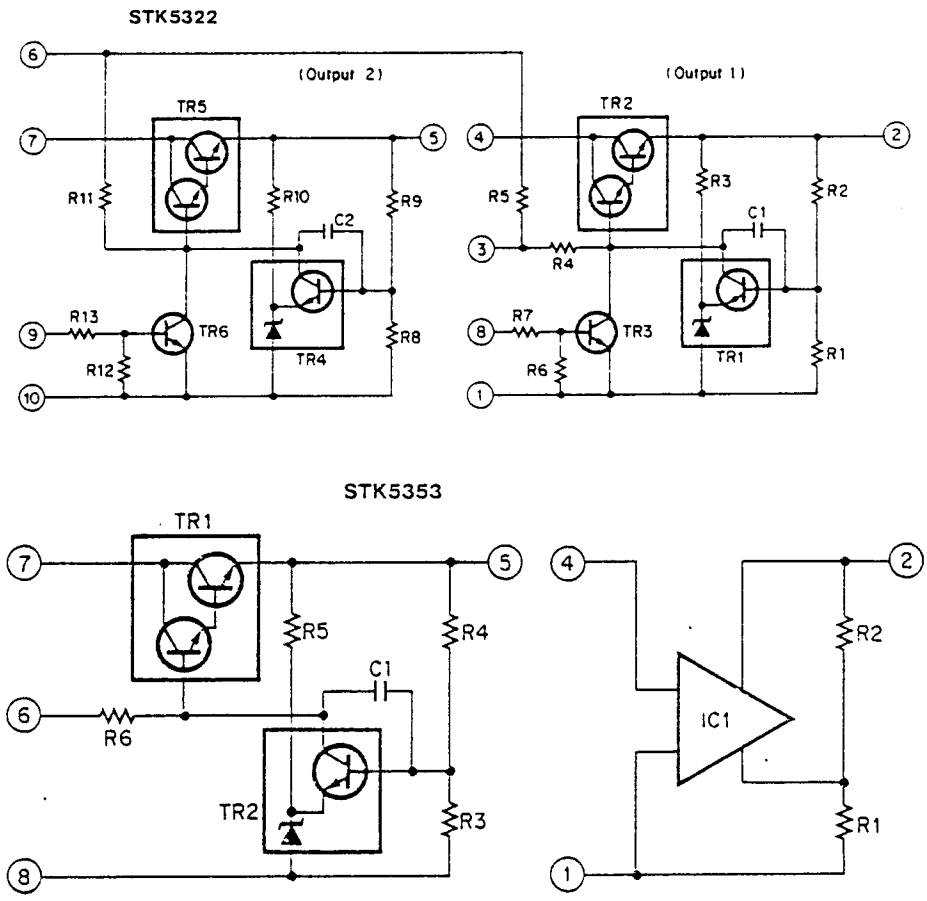
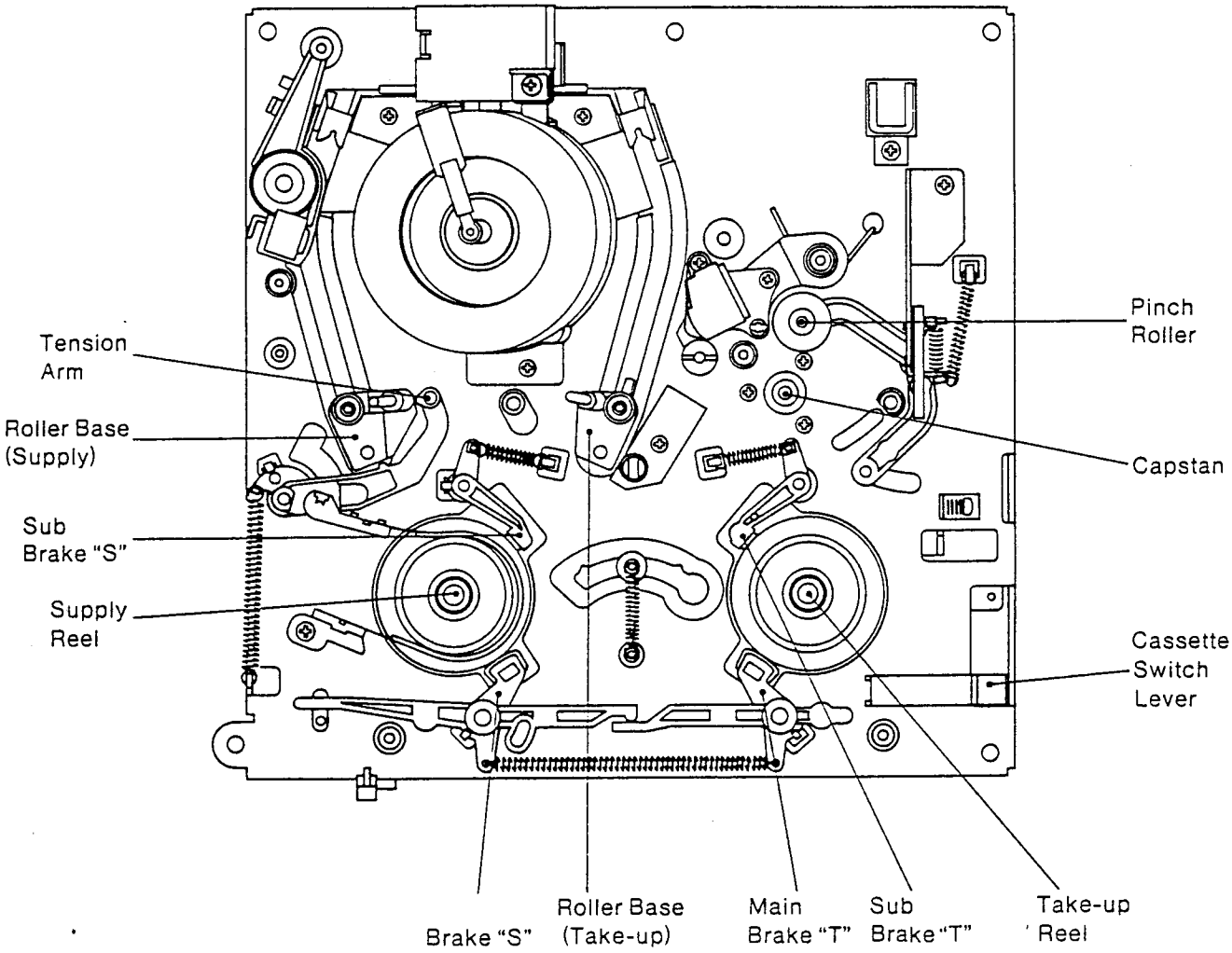


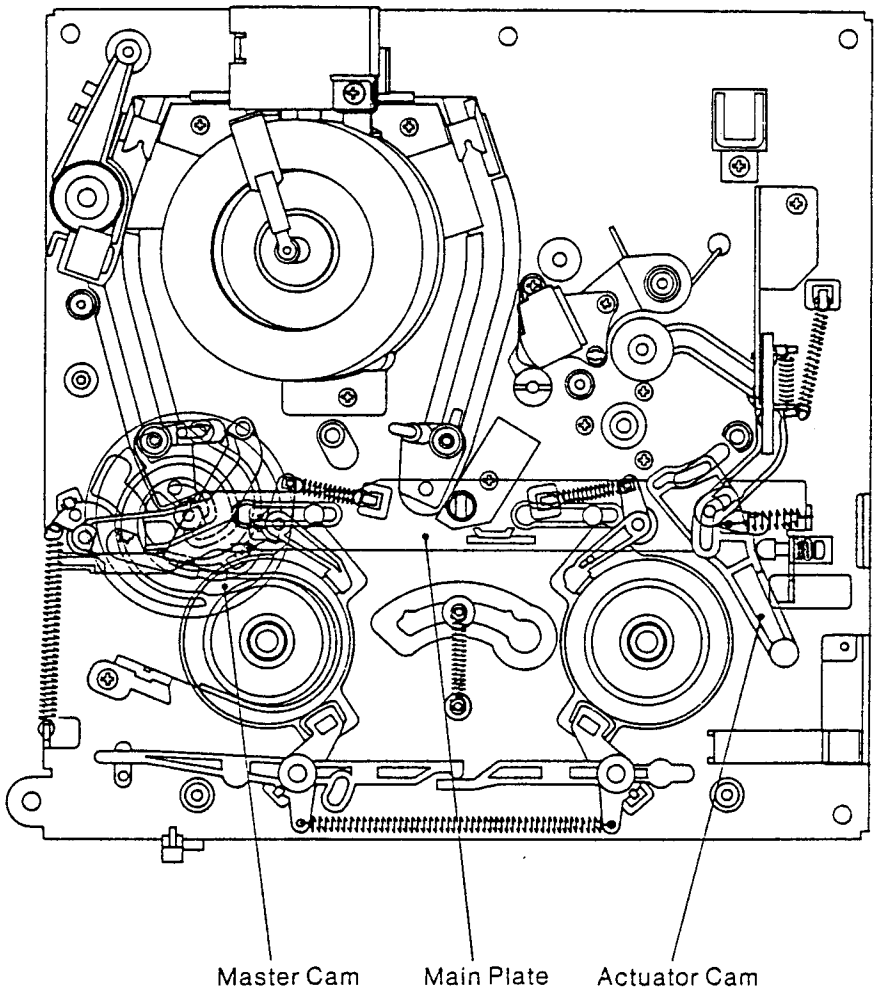
Fig. 2-7-2

3. MECHANISM DESCRIPTION

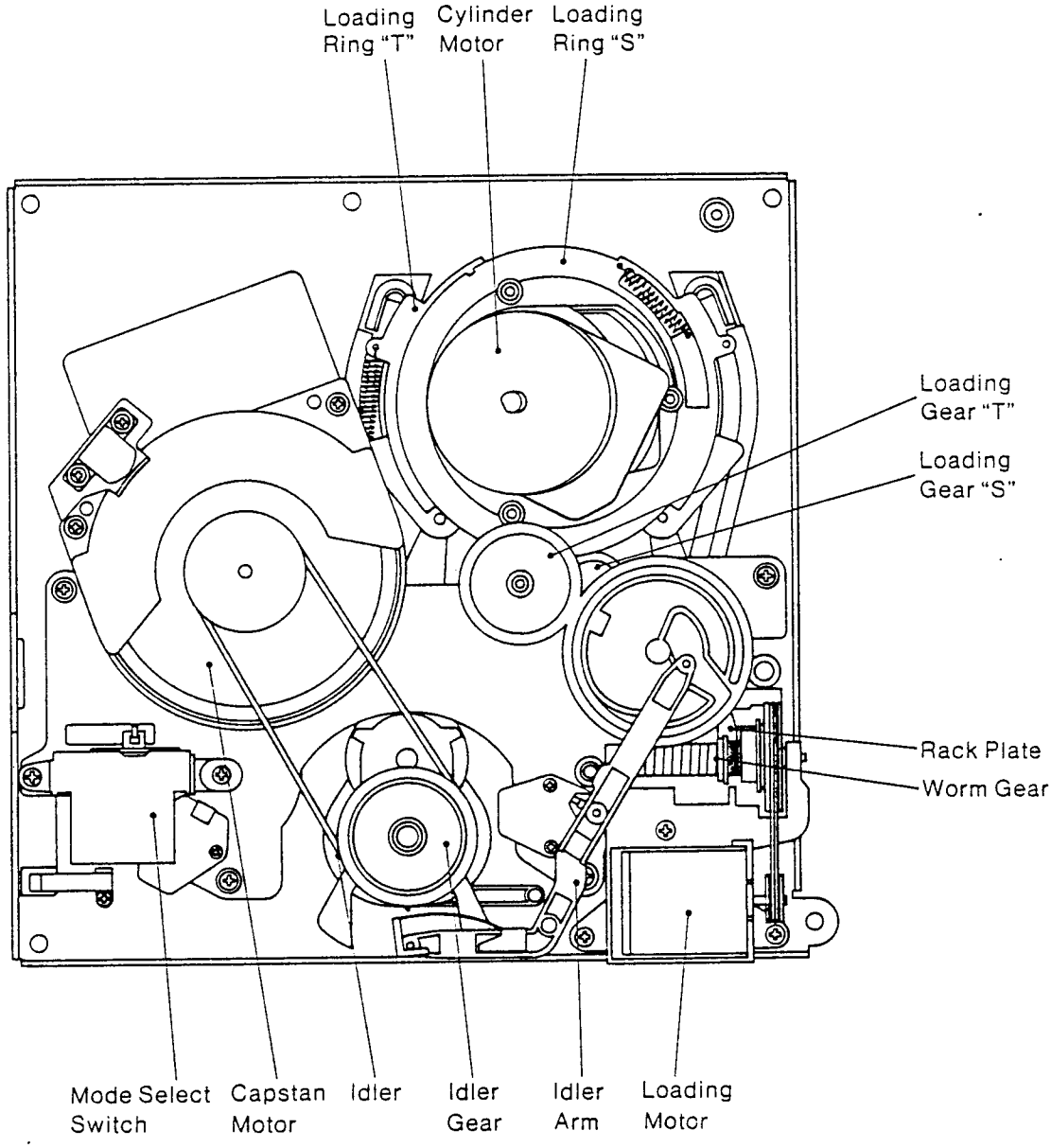
3-1. MAIN DRIVING PARTS LOCATIONS



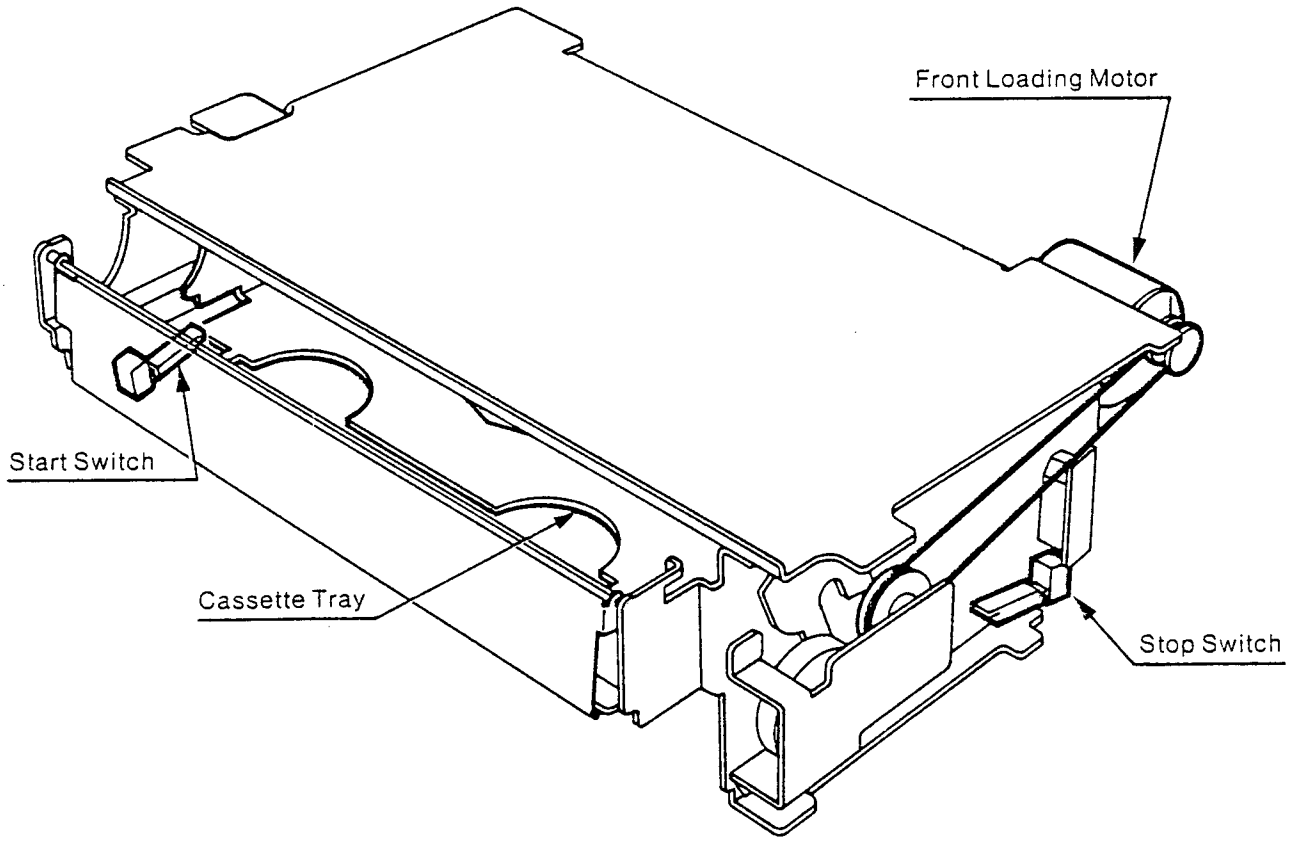
(TOP VIEW)



(TOP VIEW)

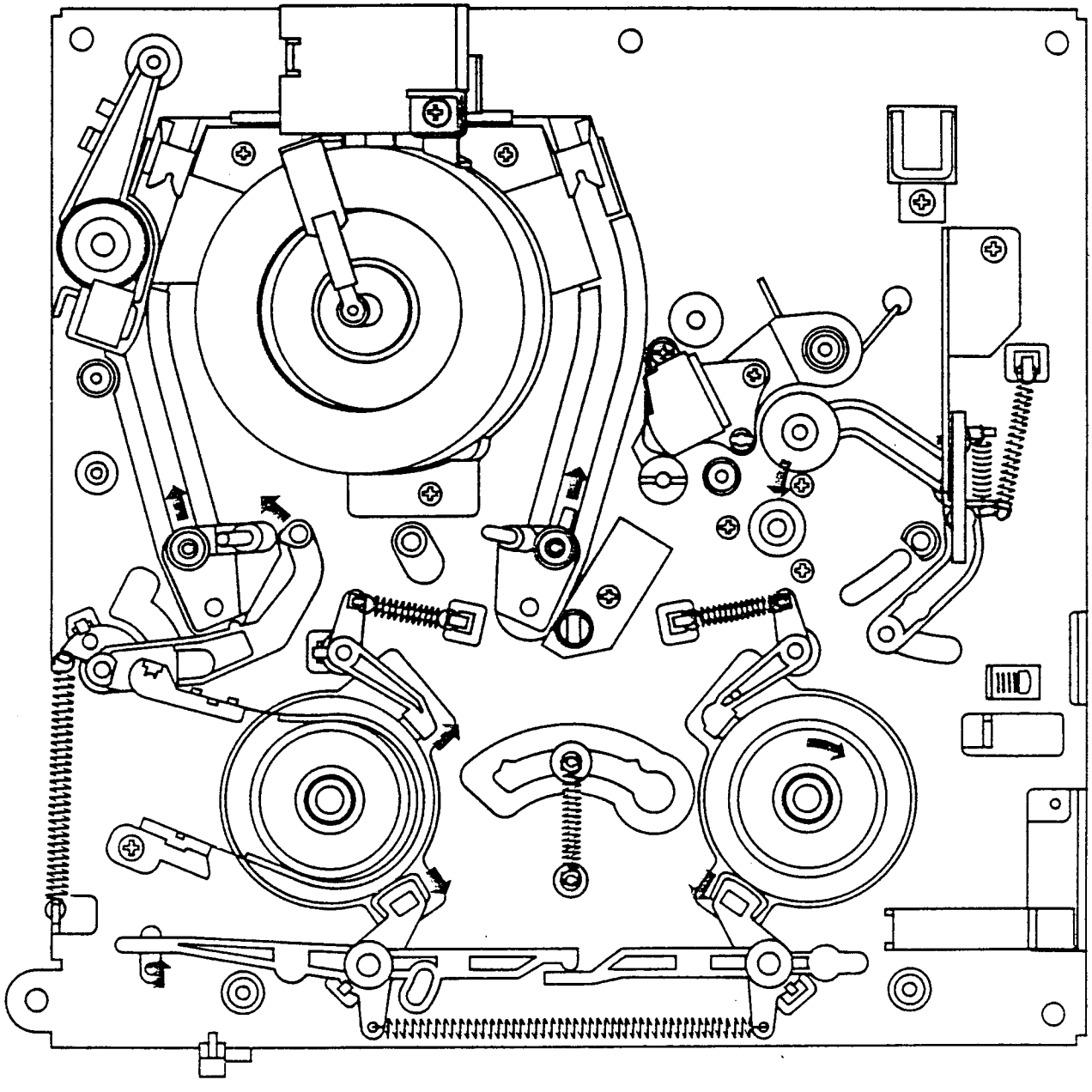

Loading Ring "T"
Cylinder Motor
Loading Ring "S"
Loading Gear "T"
Loading Gear "S"
Rack Plate
Worm Gear
Mode Select Switch
Capstan Motor
Idler
Idler Gear
Idler Arm
Loading Motor

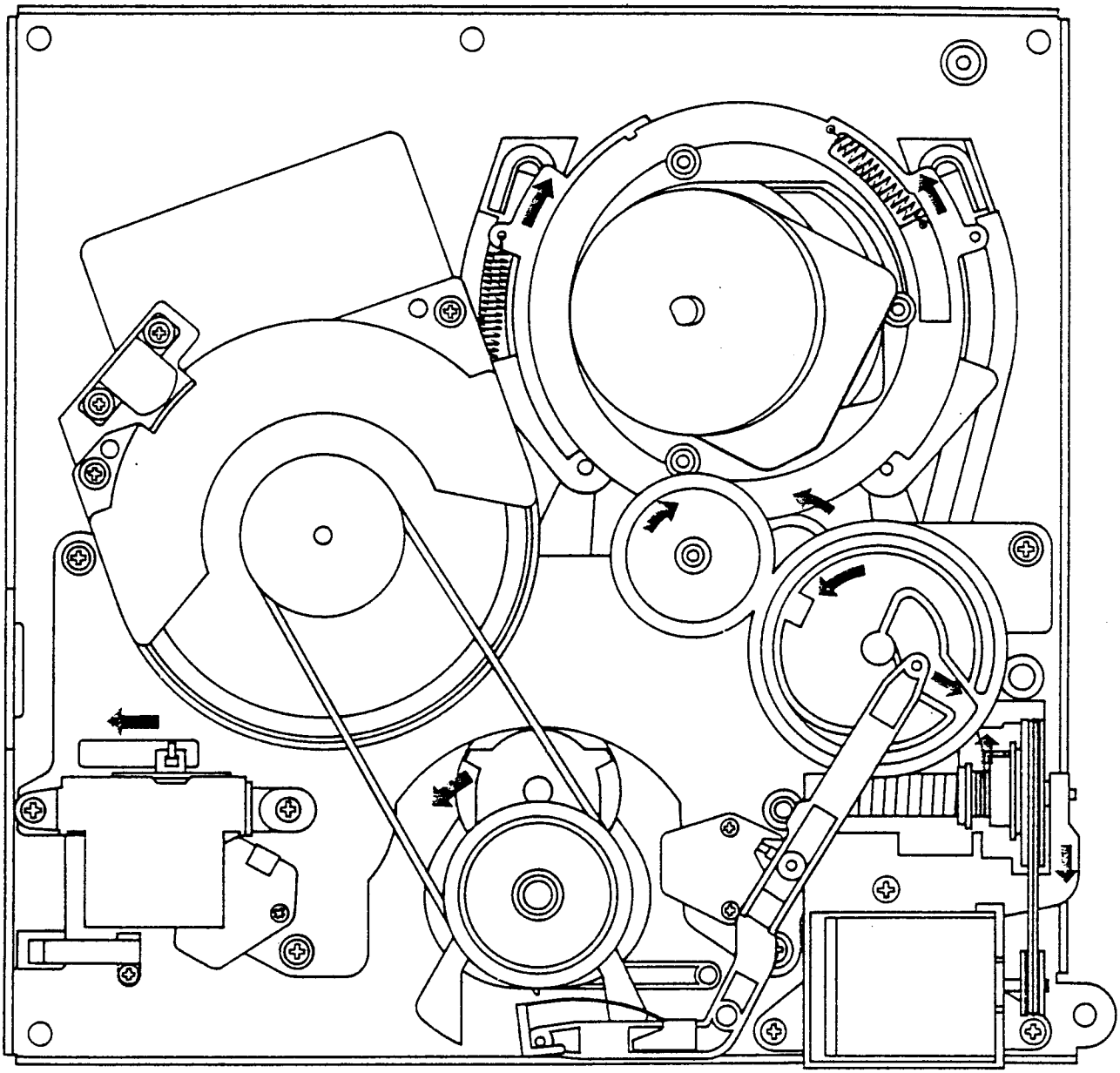
(BOTTOM VIEW)

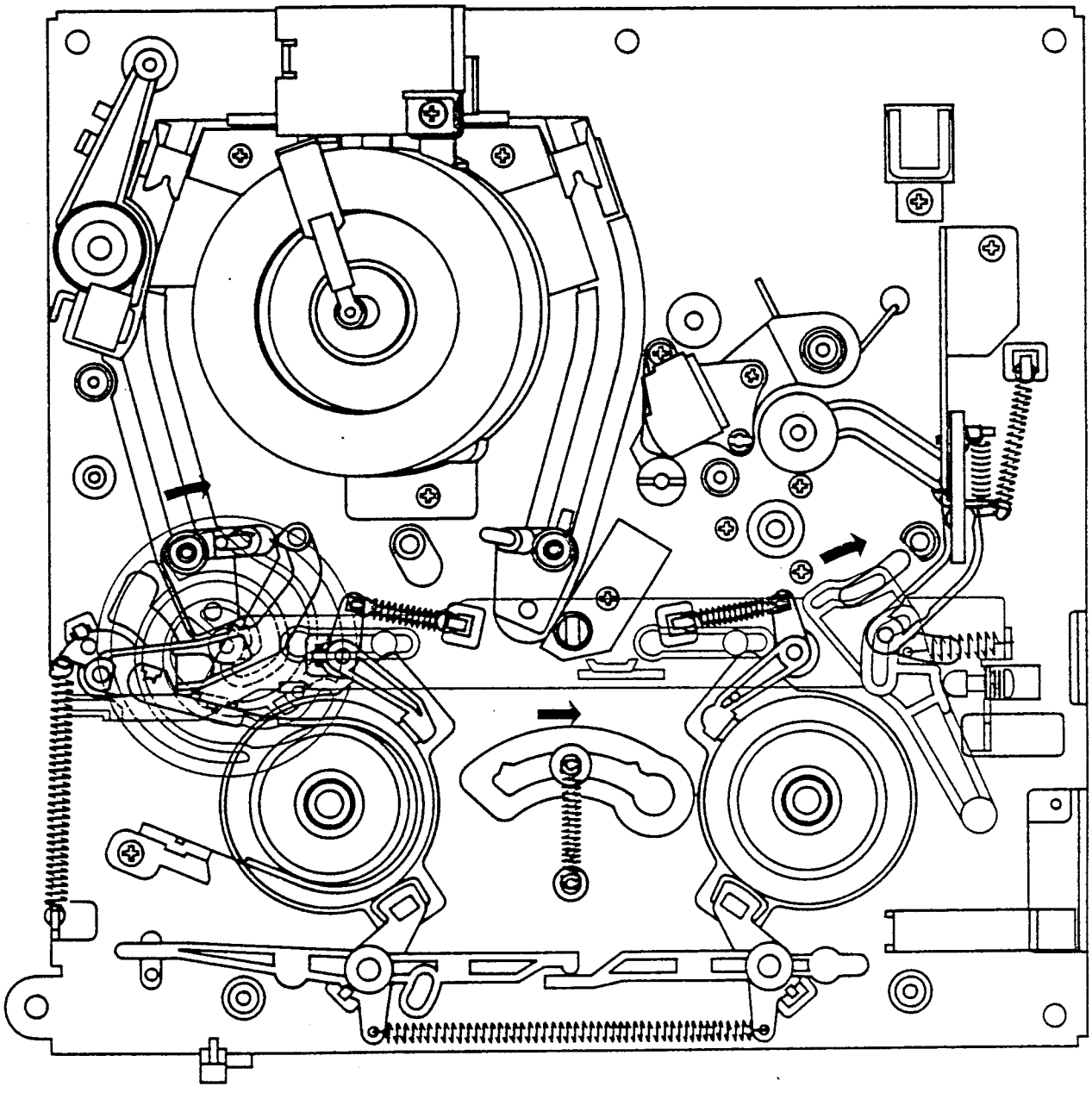


(CASSETTE HOLDER MECHANISM)

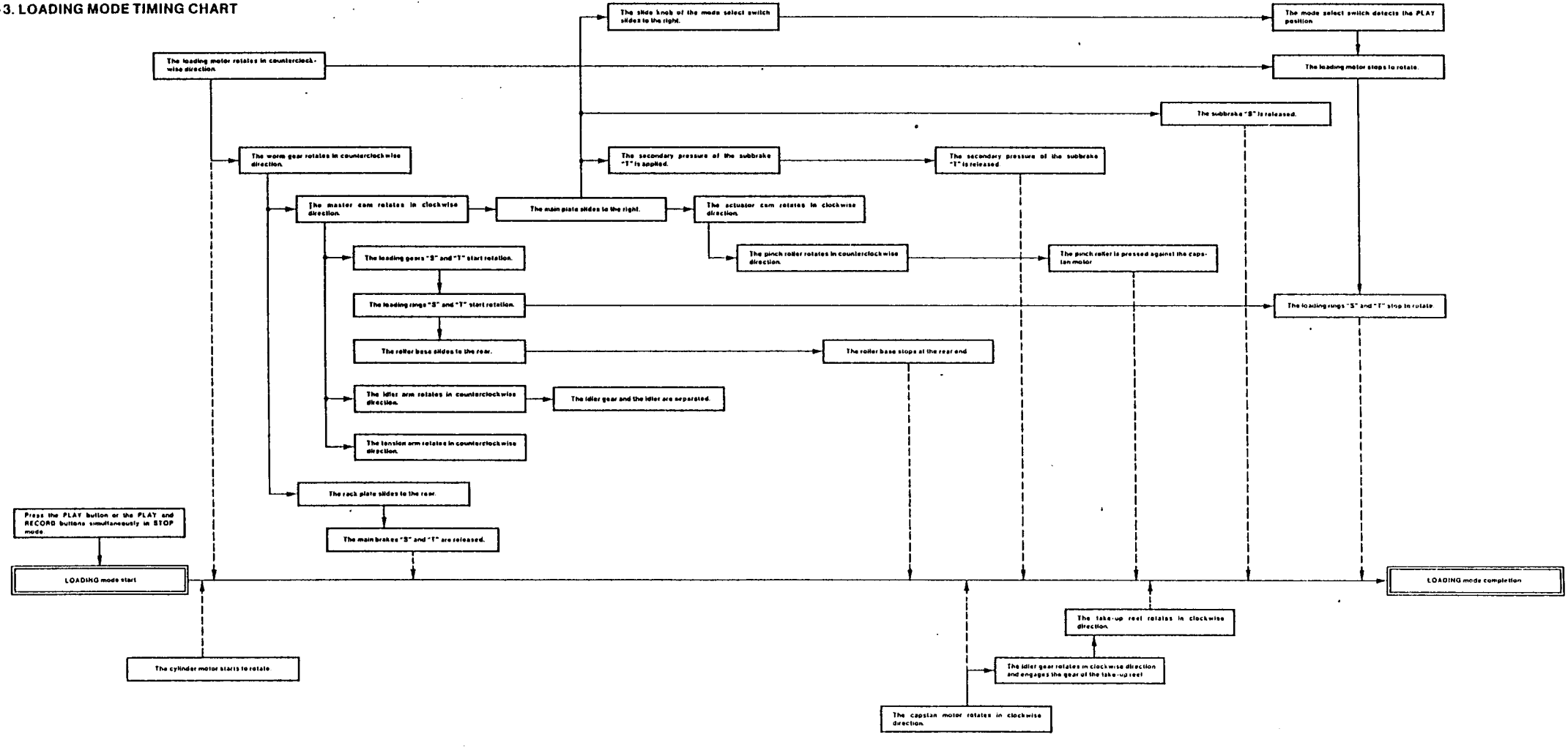
3-2. LOADING MODE OPERATION



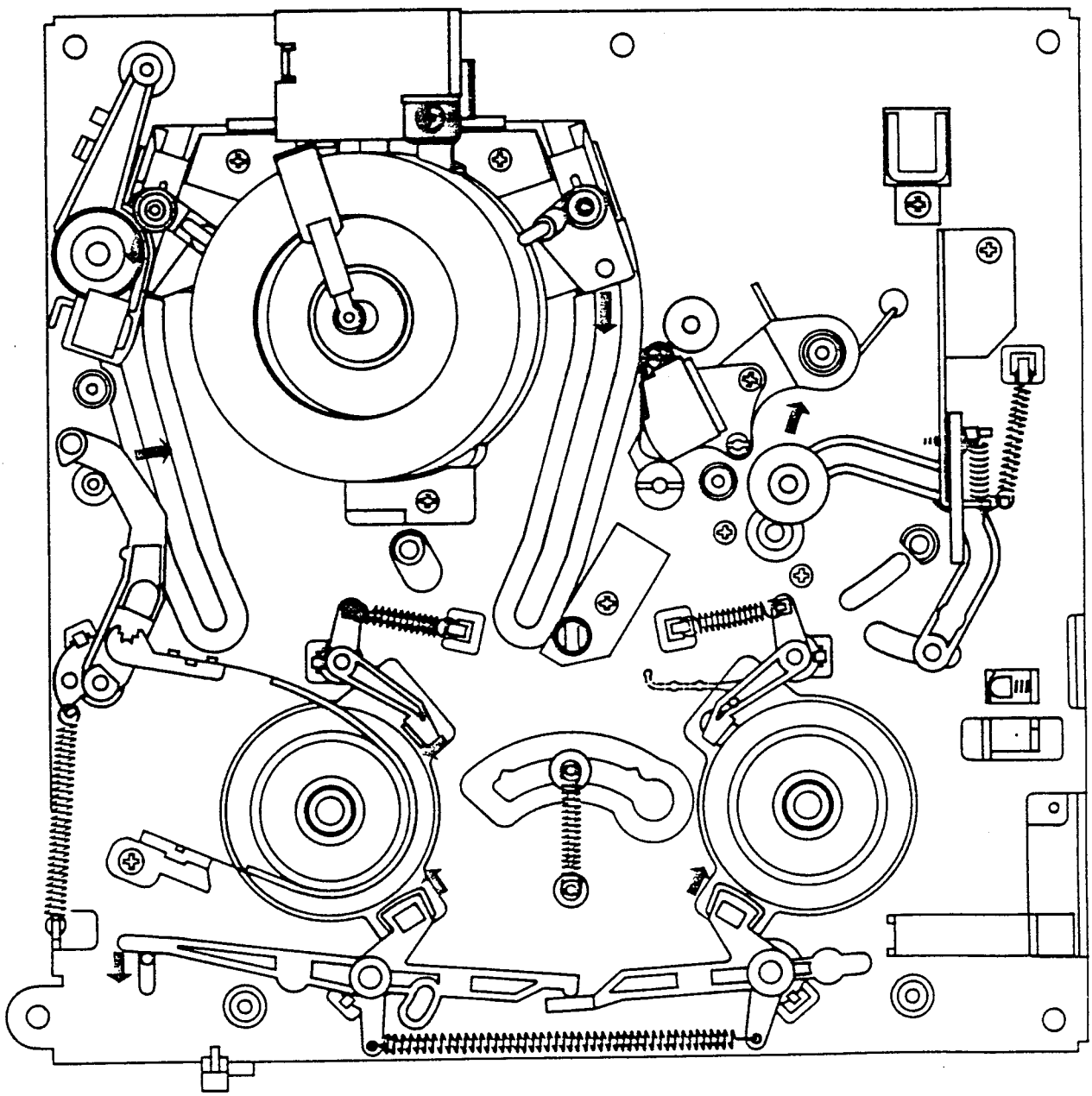


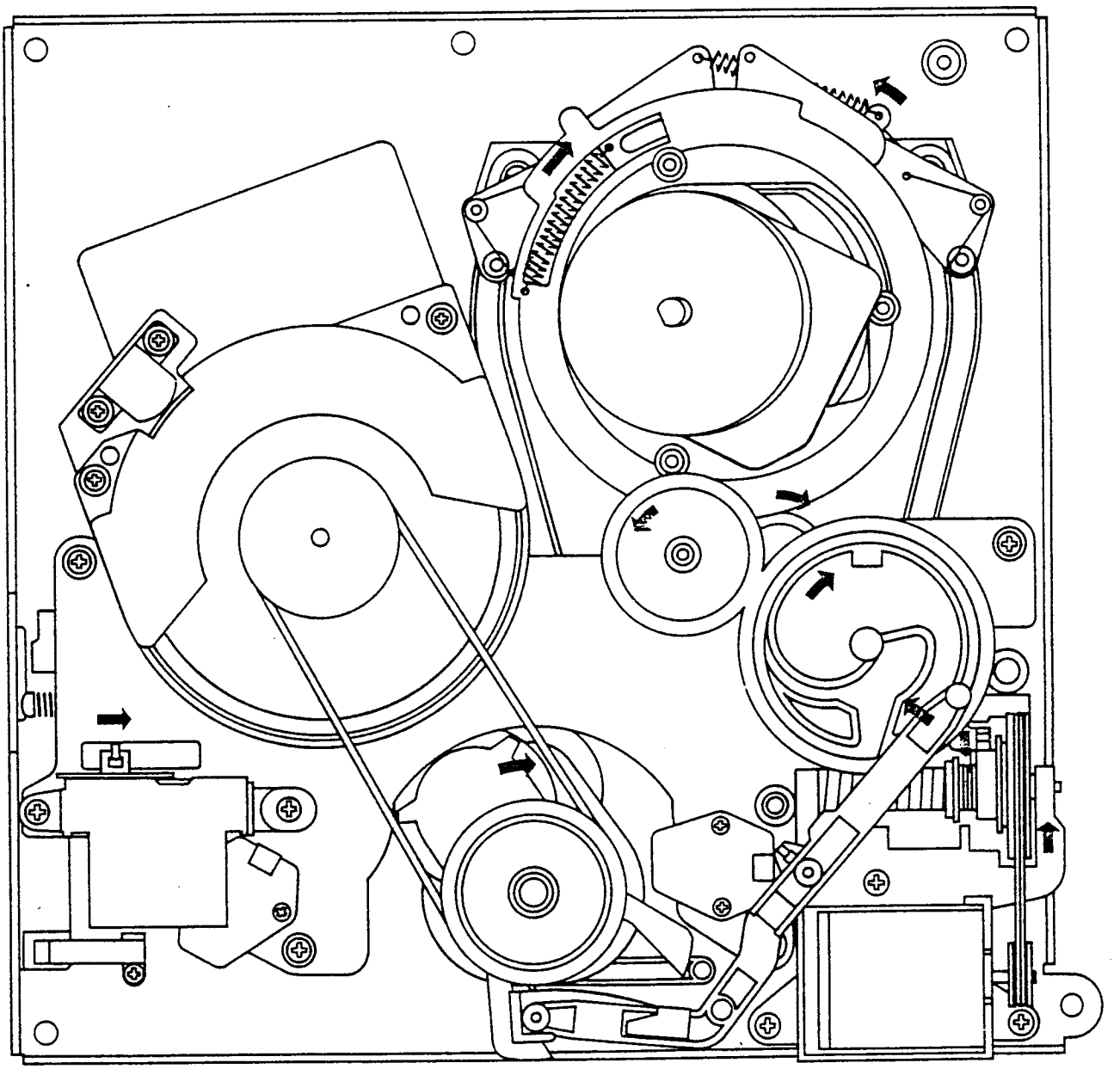


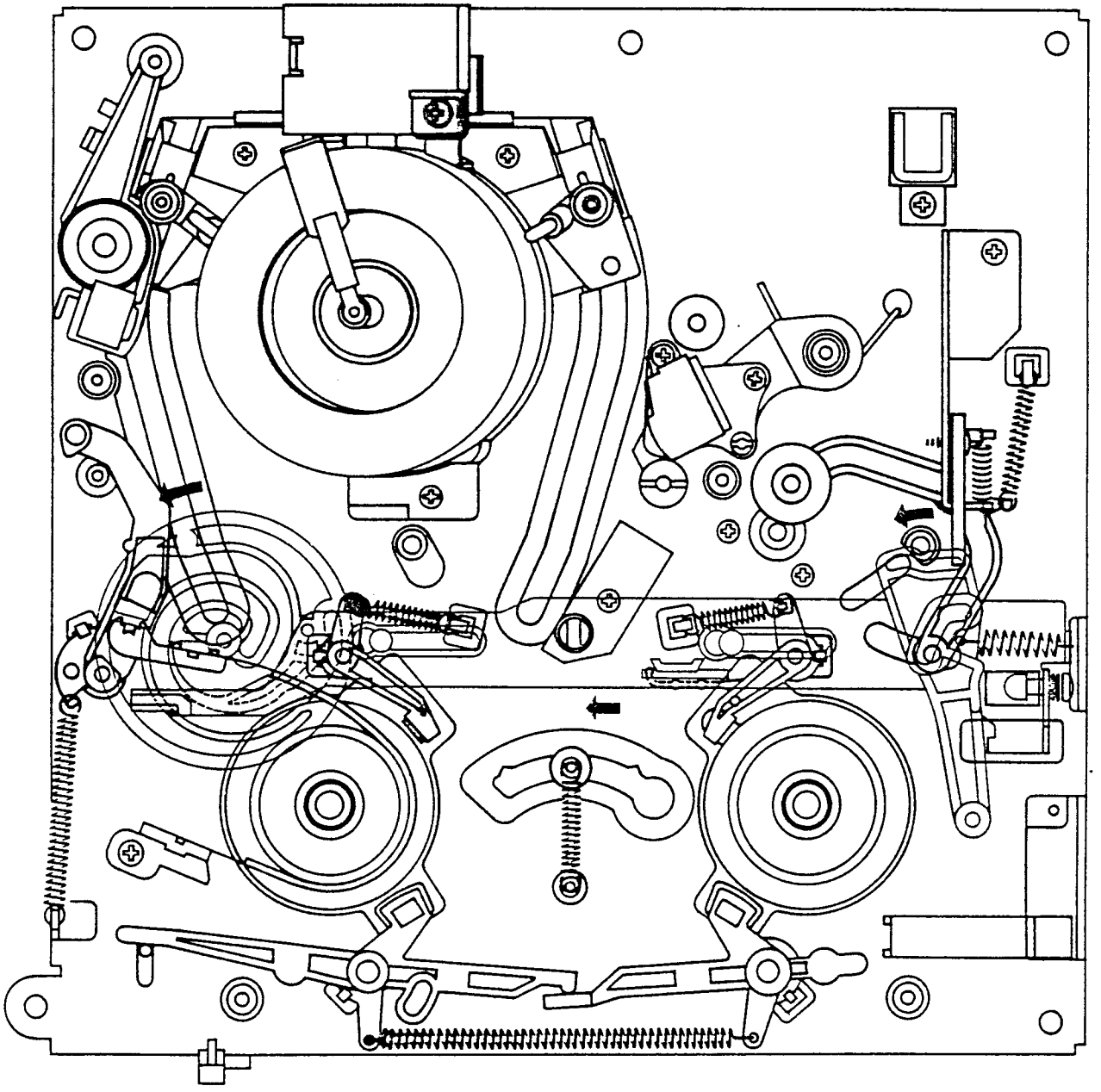
3-3. LOADING MODE TIMING CHART



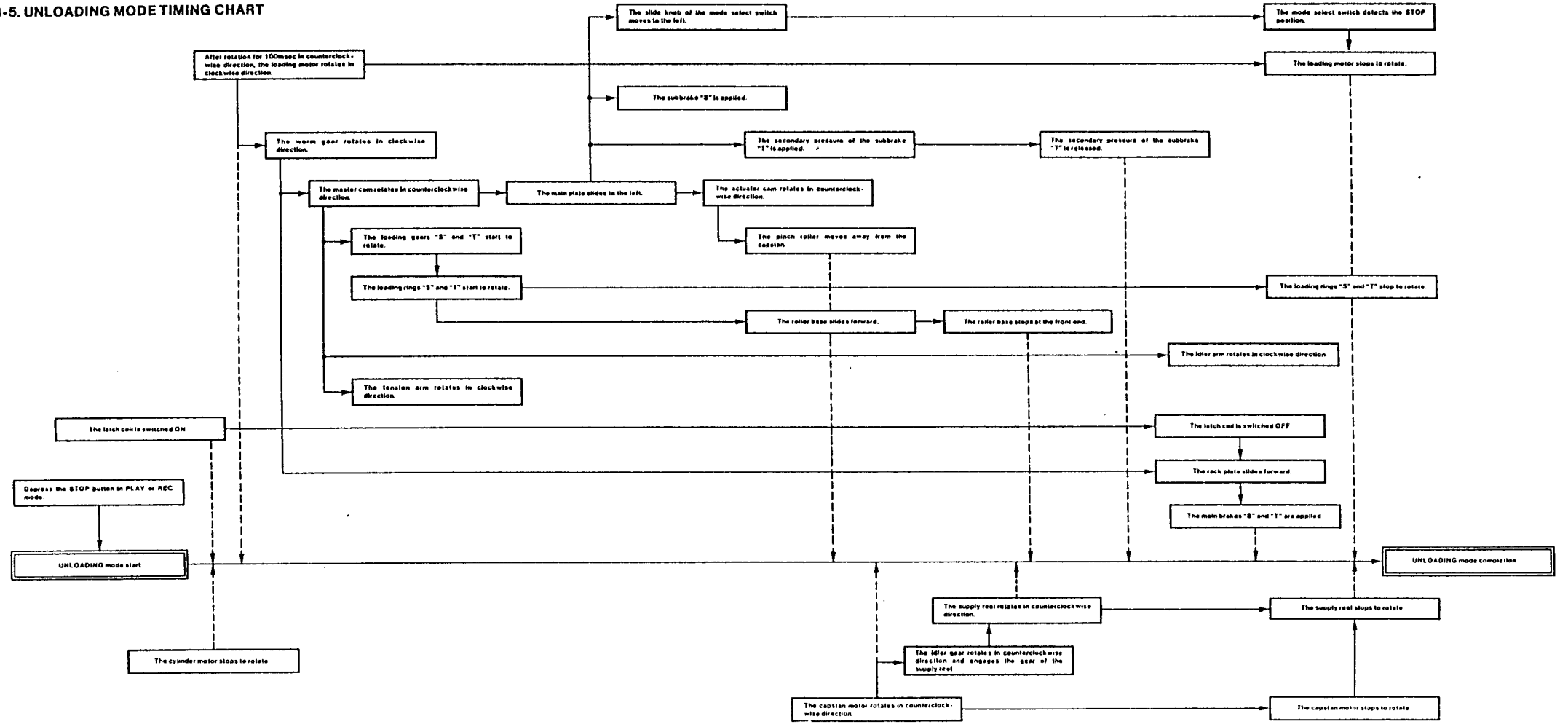
3-4. UNLOADING MODE OPERATION



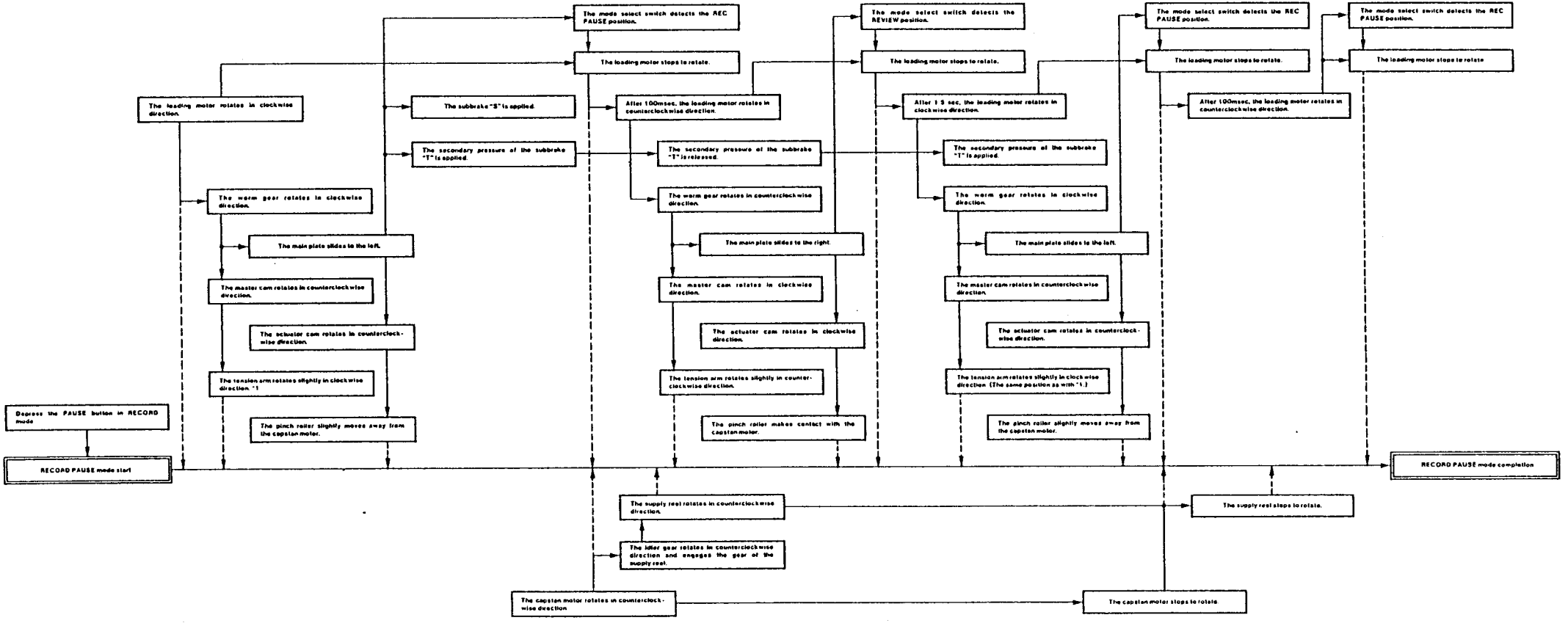




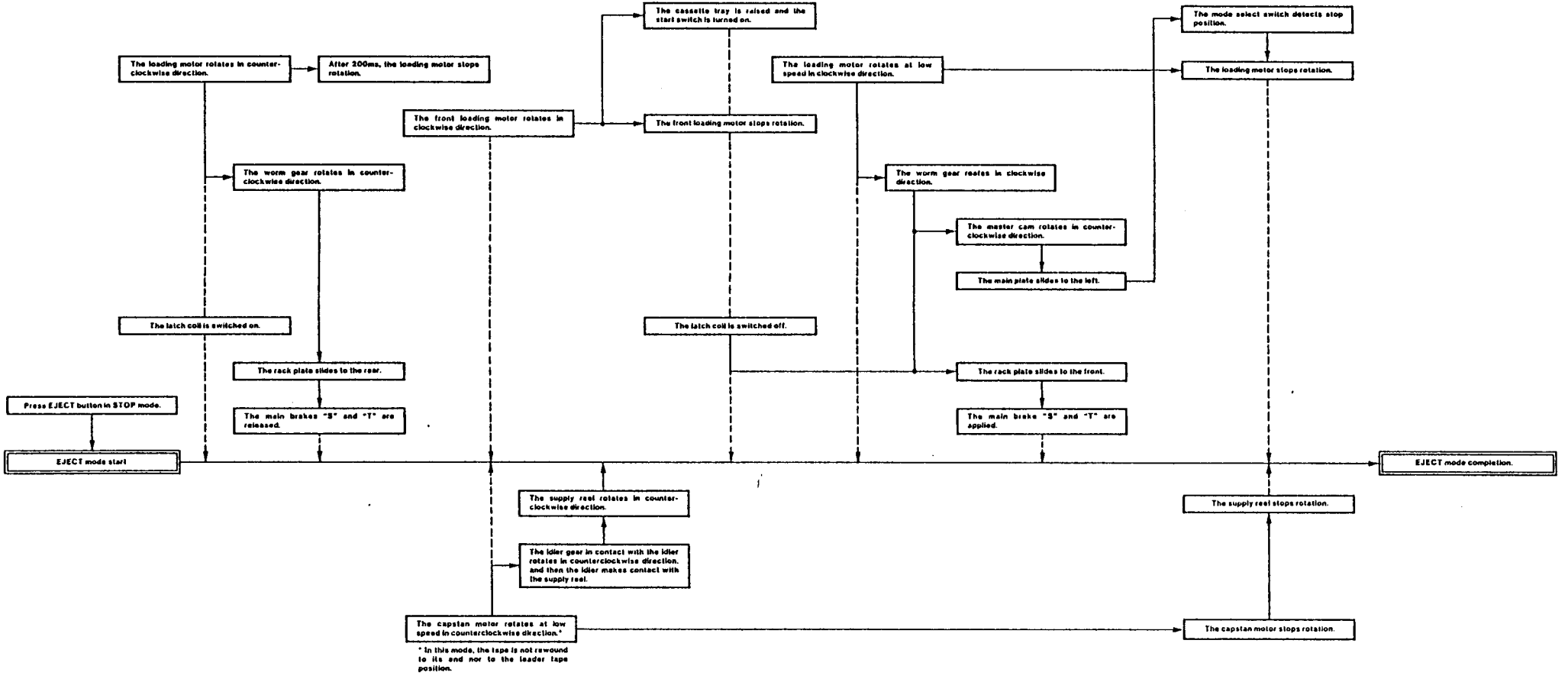
3-5. UNLOADING MODE TIMING CHART



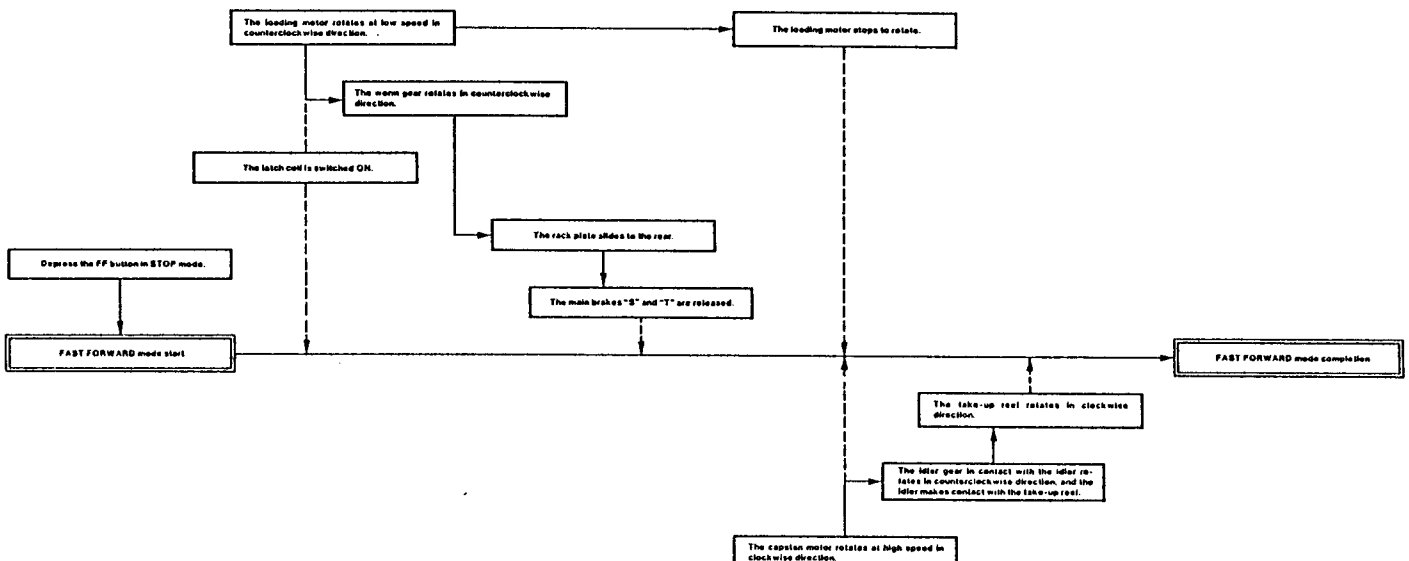
3-6. REC PAUSE MODE TIMING CHART



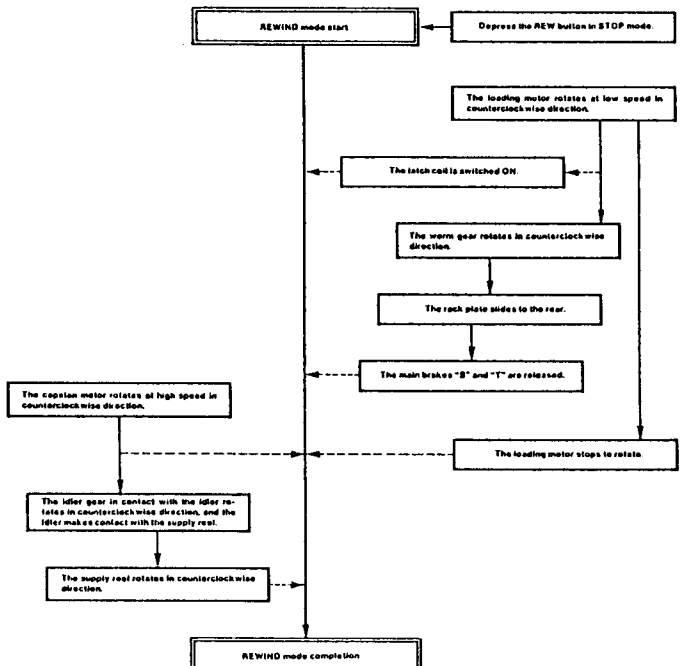
3-7. EJECT MODE TIMING CHART



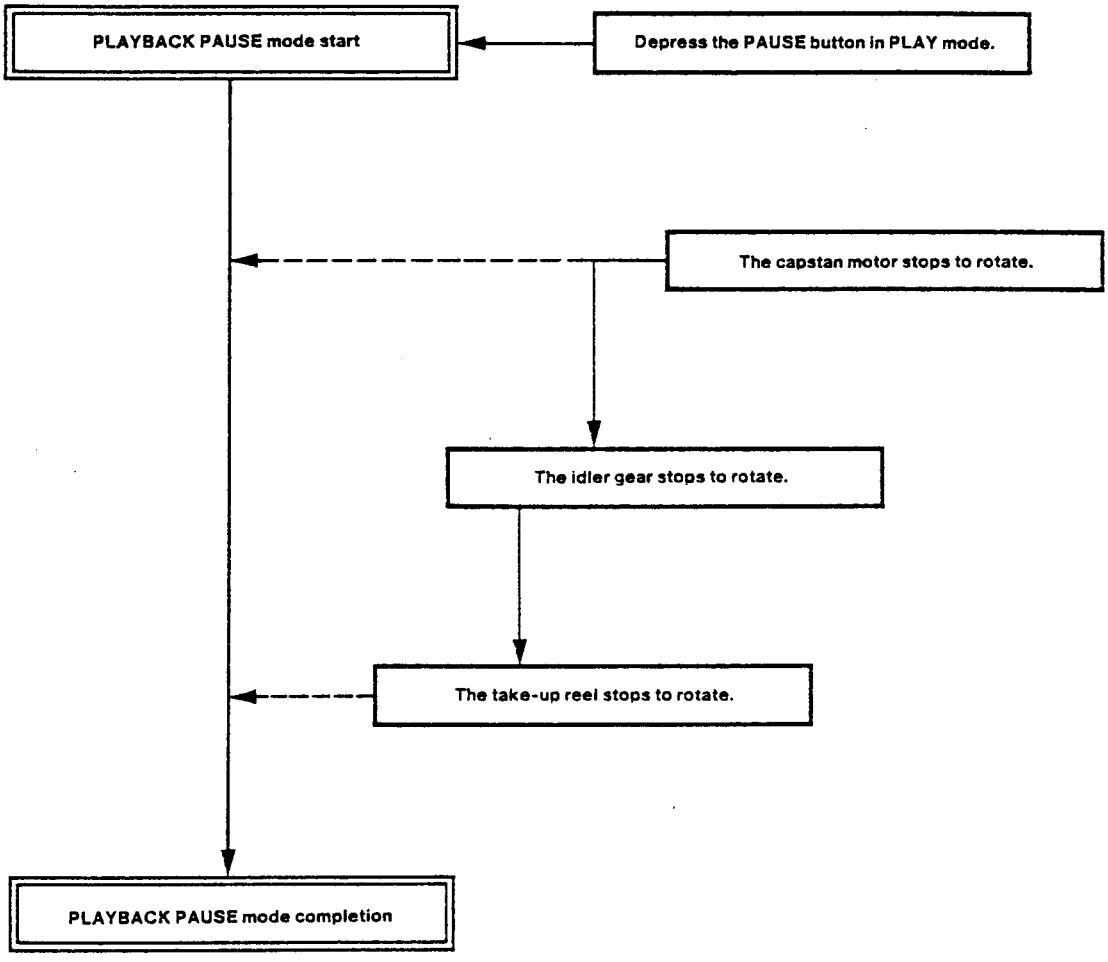
-8. FAST FORWARD MODE TIMING CHART



3-9. REWIND MODE TIMING CHART



3-10. PLAY PAUSE MODE TIMING CHART



3-11. CONDITION OF EACH MODE

DESCRIPTION / MODE	CYLINDER MOTOR	CAPSTAN MOTOR	LOADING MOTOR	MAIN BRAKE S	MAIN BRAKE T	SUB BRAKE S	SUB BRAKE T		MODE SELECT SWITCH
							P. R.	S. R.	
STOP	OFF	OFF	OFF	ON	ON	ON	ON	OFF	STOP
LOADING	ON	OFF→ ON (CW)	ON (CCW)	OFF	OFF	ON→ OFF	ON	OFF→ ON→ OFF	
UNLOADING	OFF	ON (CCW)	ON (CW)	OFF	OFF	OFF→ ON	ON	OFF→ ON→ OFF	
FAST FORWARD	OFF	ON (CW)	OFF	OFF	OFF	ON	ON	OFF	STOP
REWIND	OFF	ON (CCW)	OFF	OFF	OFF	ON	ON	OFF	STOP
PLAY	ON	ON (CW)	OFF	OFF	OFF	OFF	ON	OFF	PLAY
CUE	ON	ON (CW)	OFF	OFF	OFF	OFF	ON	OFF	PLAY
REVIEW	ON	ON (CCW)	OFF	OFF	OFF	ON	ON	OFF	REVIEW
PB PAUSE	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	PLAY
REC	ON	ON (CW)	OFF	OFF	OFF	OFF	ON	OFF	PLAY
REC PAUSE	ON	OFF	OFF	OFF	OFF	ON	ON	ON	REC PAUSE
EJECT	OFF	ON (CCW)	ON→ OFF	ON→ OFF	ON→ OFF	ON	ON	OFF	EJECT

NOTES:
P.R. = Primary pressure ..... 30 gr-cm.
S.R. = Secondary pressure ..... 60 gr-cm.
CW = Clockwise.
CCW = Counterclockwise.

4. MAINTENANCE

4-1. MAINTENANCE PARTS AND PERIODS

In order to keep the VCR in peak working order, care for the parts indicated in Table 4-1-1 at the periods given.

Parts \ Hours	500	1000	1500	2000	2500	3000	3500	4000	5000
CYLINDER	○	○	○	○	○	○	○	○	○
AUDIO CONTROL HEAD	○	○	○	○	○	○	○	○	○
FULL ERASE HEAD	○	○	○	○	○	○	○	○	○
CAPSTAN MOTOR	○	○	○	○	○	○	○	○	○
PINCH ROLLER	○	○	○	○	○	○	○	○	○
TAKE-UP REEL				▲			▲		
SUPPLY REEL				▲			▲		

○ : Cleaning ... Freon (fluorine-based organic solvent) absolute methyl alcohol
▲ : Lubrication ... Oil (Turbionol No. 64 or equivalent)

Table 4-1-1

4-2. CLEANING

4-2-1. CYLINDER

Wrap a piece of chamois around your finger. Dip it in head-cleaning fluid and clean the cylinder head. Move the chamois horizontally several times (in the direction of the arrow). Another cylinder head is located 180° on the opposite side. Clean it in the same way.
In same manner, clean the tape transport area of the cylinder. (See Fig. 4-2-1)
NOTE:
Do not push forcefully against the cylinder head. Do not move it up or down since it will be damaged. Always use a piece of chamois for cleaning.

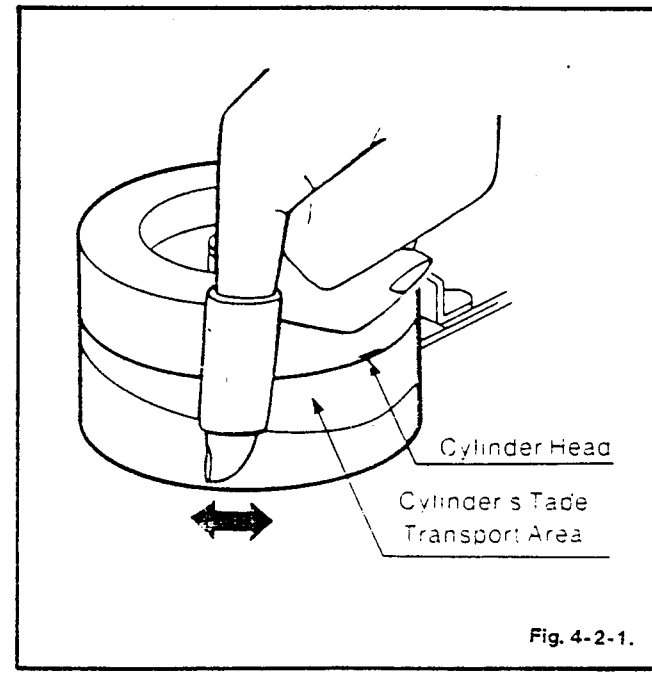


Fig. 4-2-1.

4-2-2. AUDIO CONTROL HEAD

Wrap a piece of chamois around your finger. Dip it in head-cleaning fluid and clean the audio control head, wiping it horizontally.
Clean the FULL ERASE HEAD, the CAPSTAN MOTOR, and the PINCH ROLLER in the same manner. (See Fig. 4-2-2)

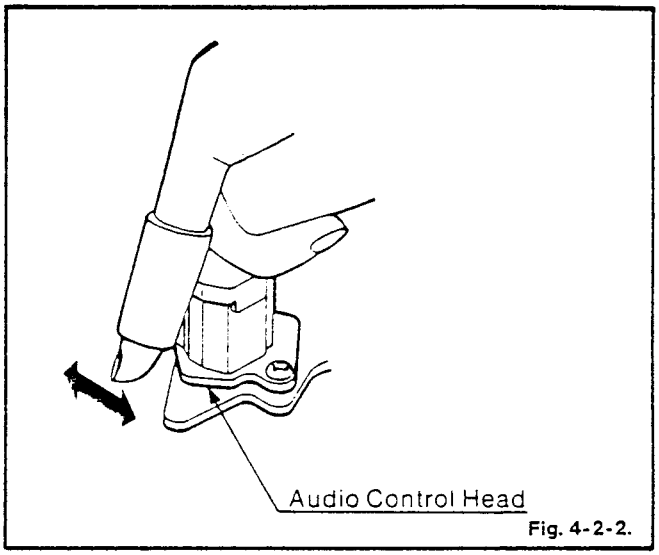


Fig. 4-2-2.

4-3. LUBRICATION

4-3-1. LUBRICATING PARTS

The following parts should be lubricated with oil (Turbinol No. 64) every 2000 hours.
(1) Supply reel
(2) Take-up reel

4-3-2. LUBRICATING PROCEDURE

(1) Detach both of the reel fix washers. (See Fig. 4-3-1)
(2) Lift the supply reel and take-up reel slightly.
(3) Apply oil to the washer and the section below the axis.
(4) Replace the supply reel and take-up reel in their normal positions, then apply oil to the section above the axis.

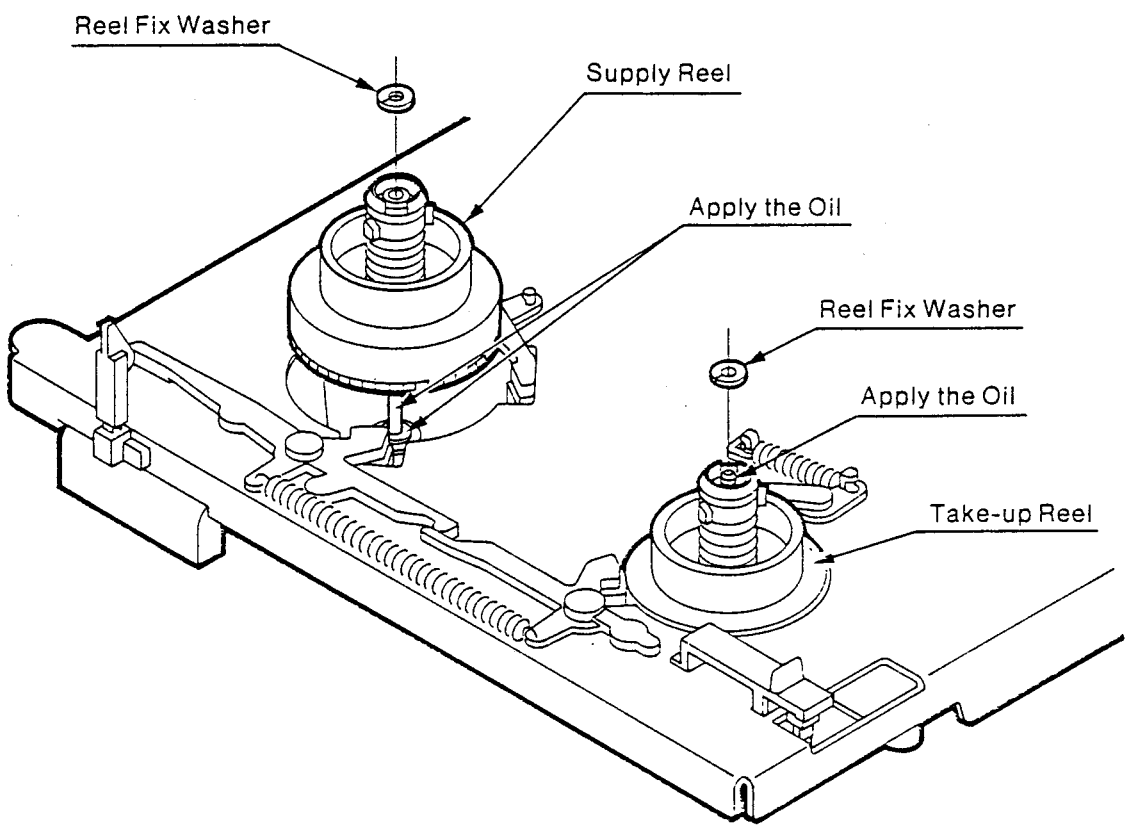
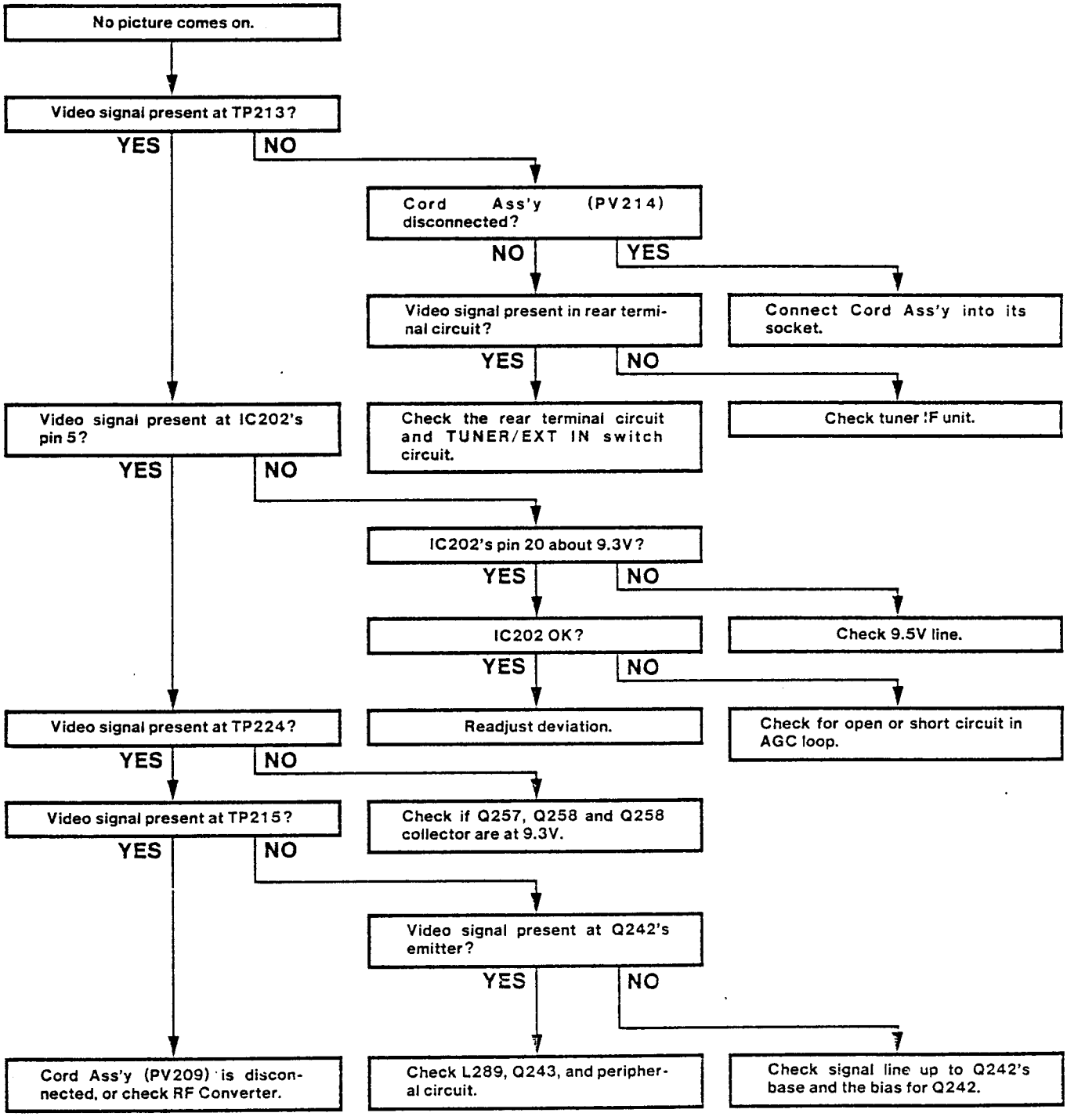


Fig. 4-3-1.

5. TROUBLE SHOOTING

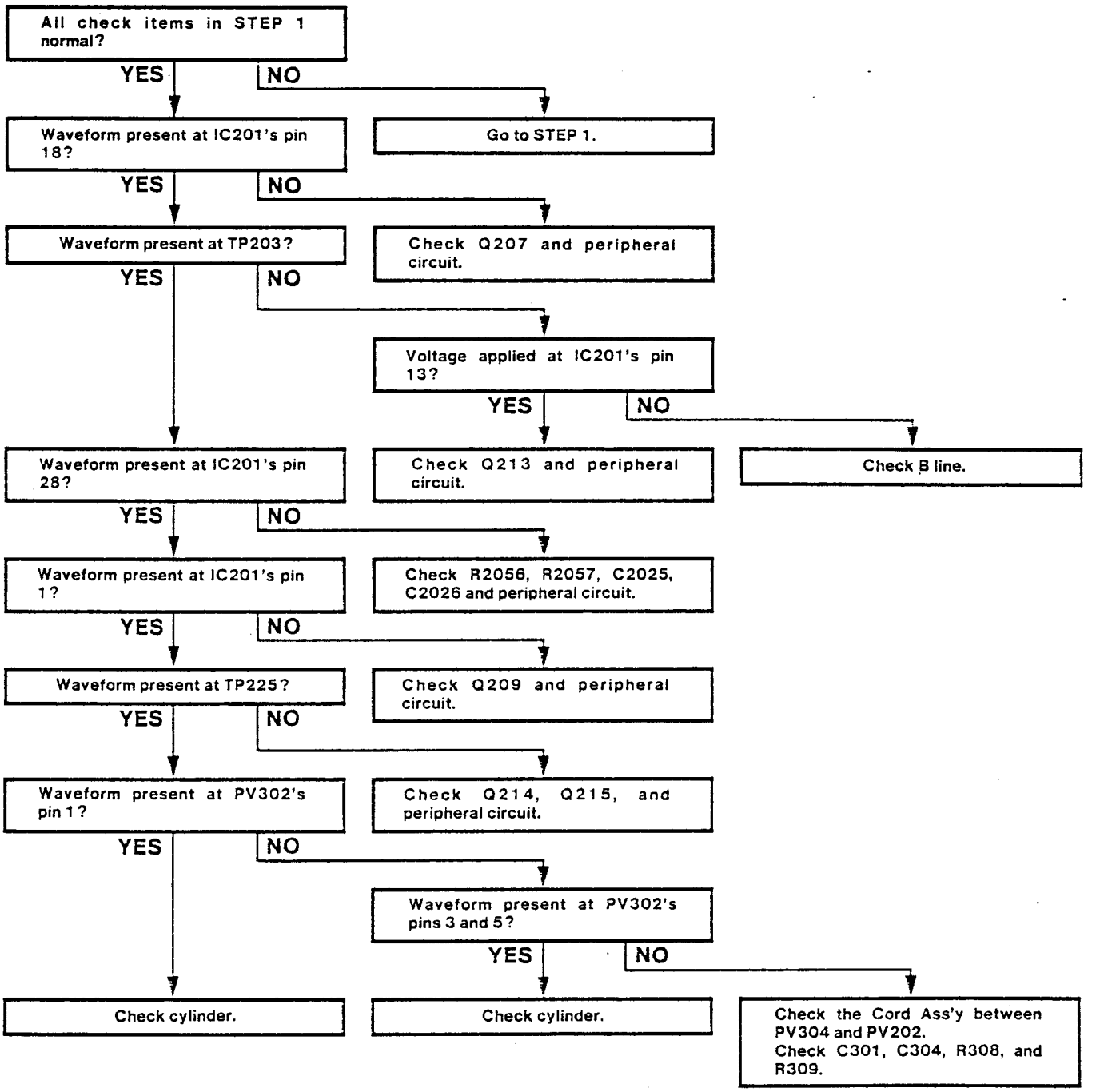
5-1. VIDEO CIRCUIT

STEP 1. E-E MODE

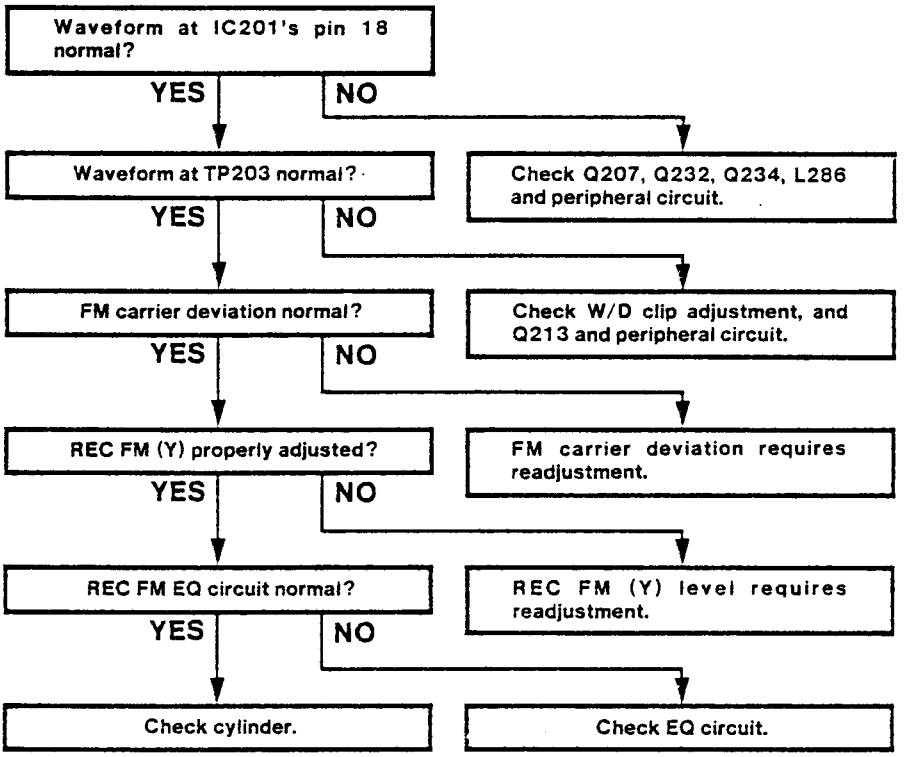


STEP 2. RECORDING MODE (LUMINANCE)

1. Picture recording failure.

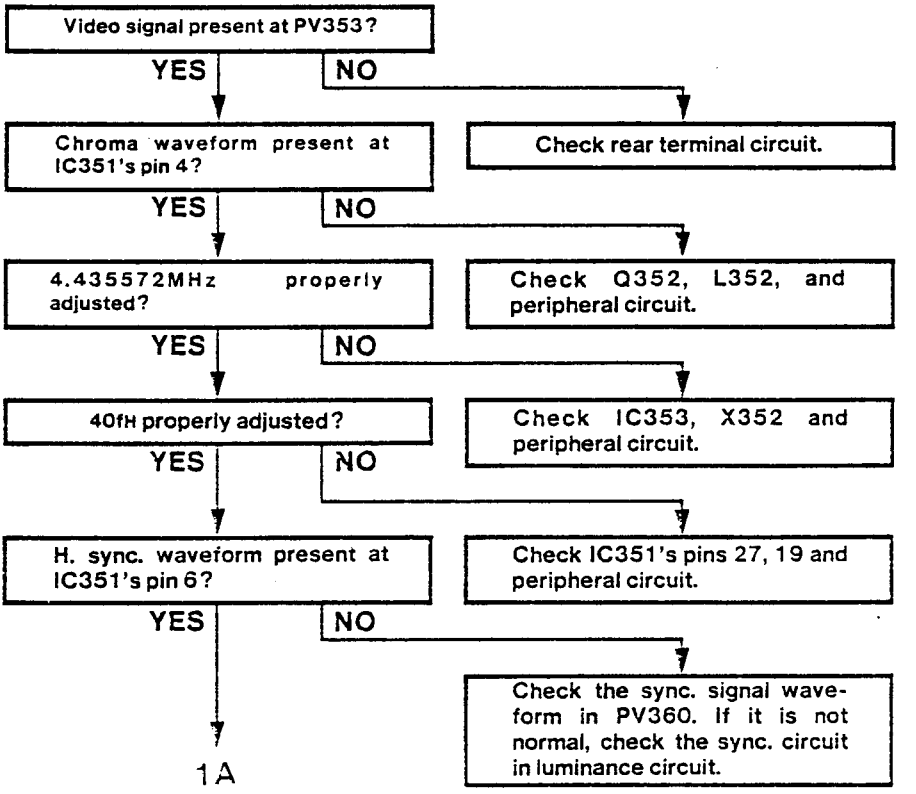


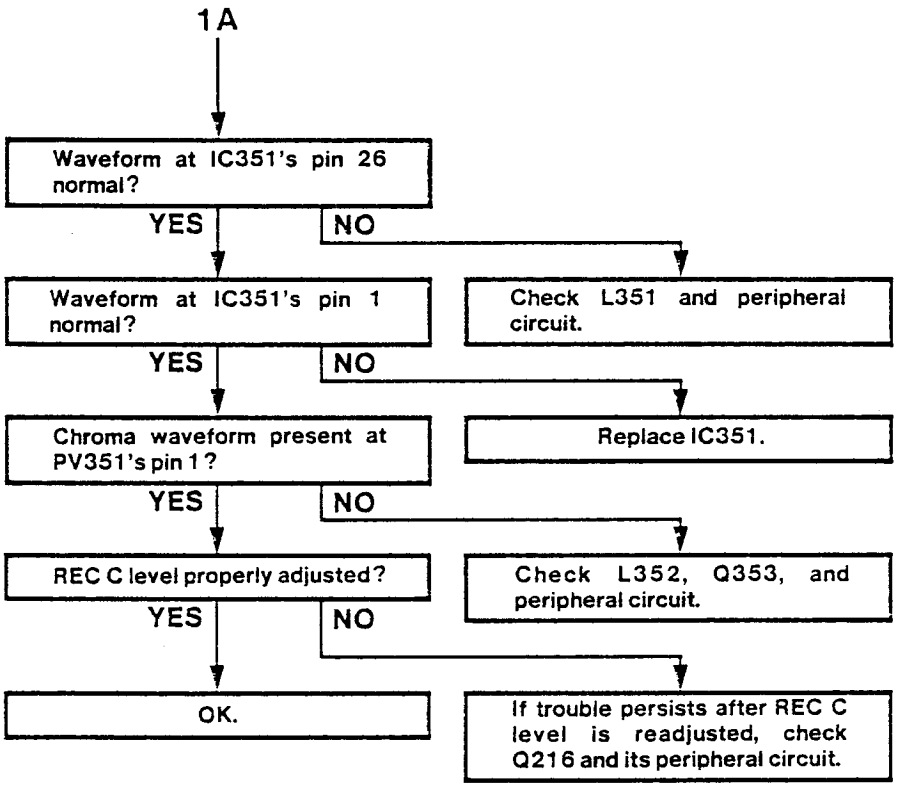
2. Smear or reverse video appears.



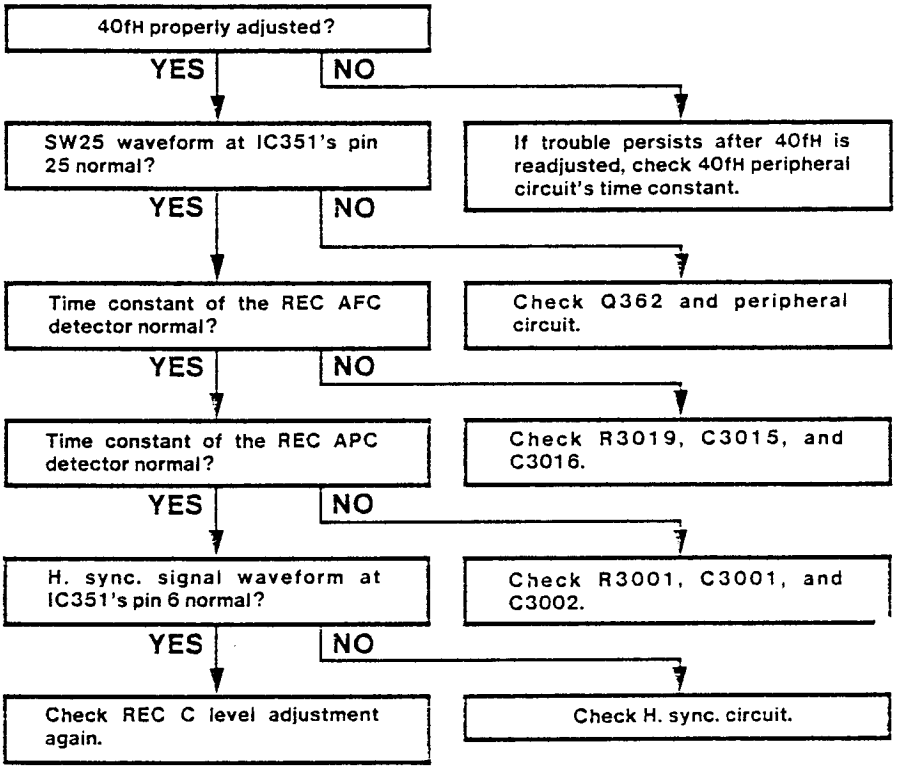
STEP 3. RECORDING MODE (CHROMIONANCE)

1. Picture completely discolored.



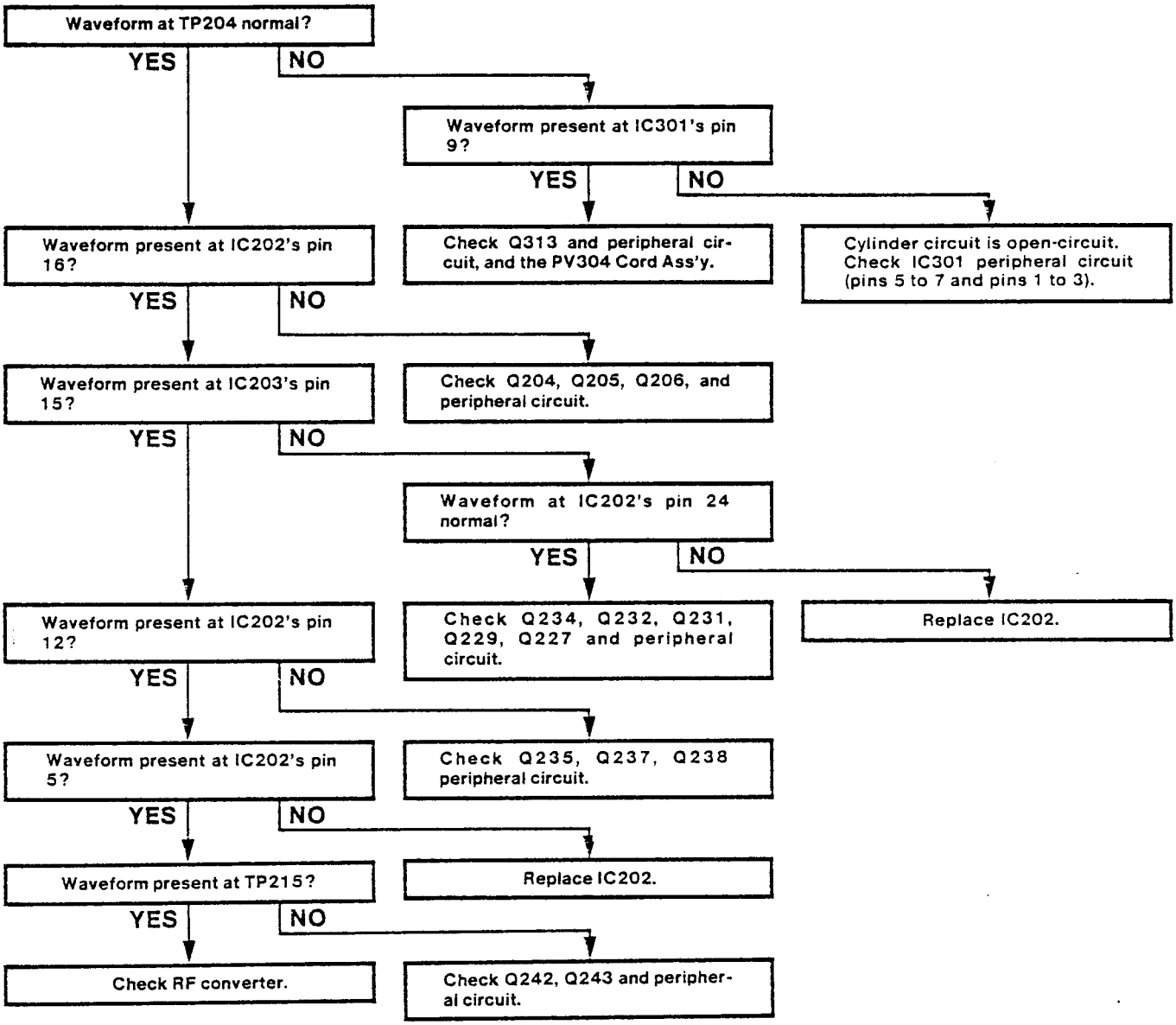


2. Improper color reproduction.

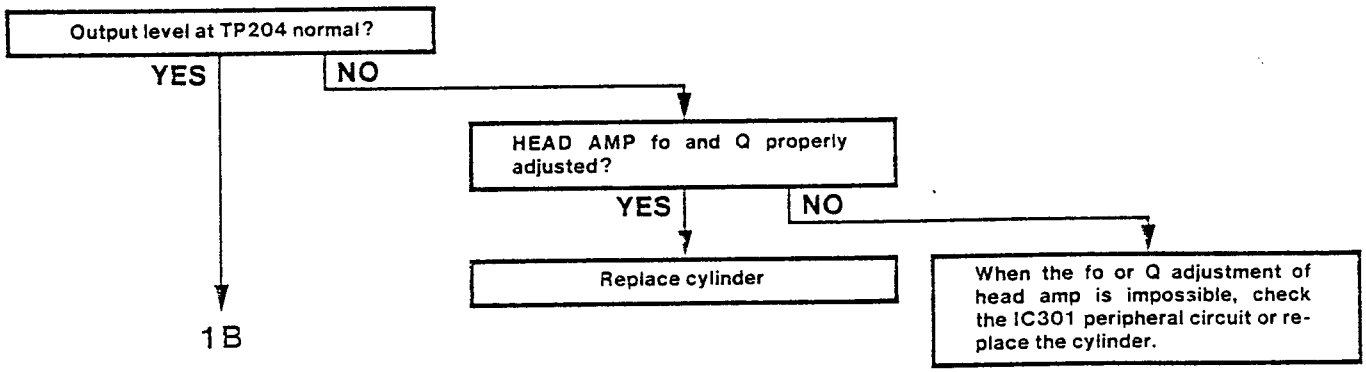


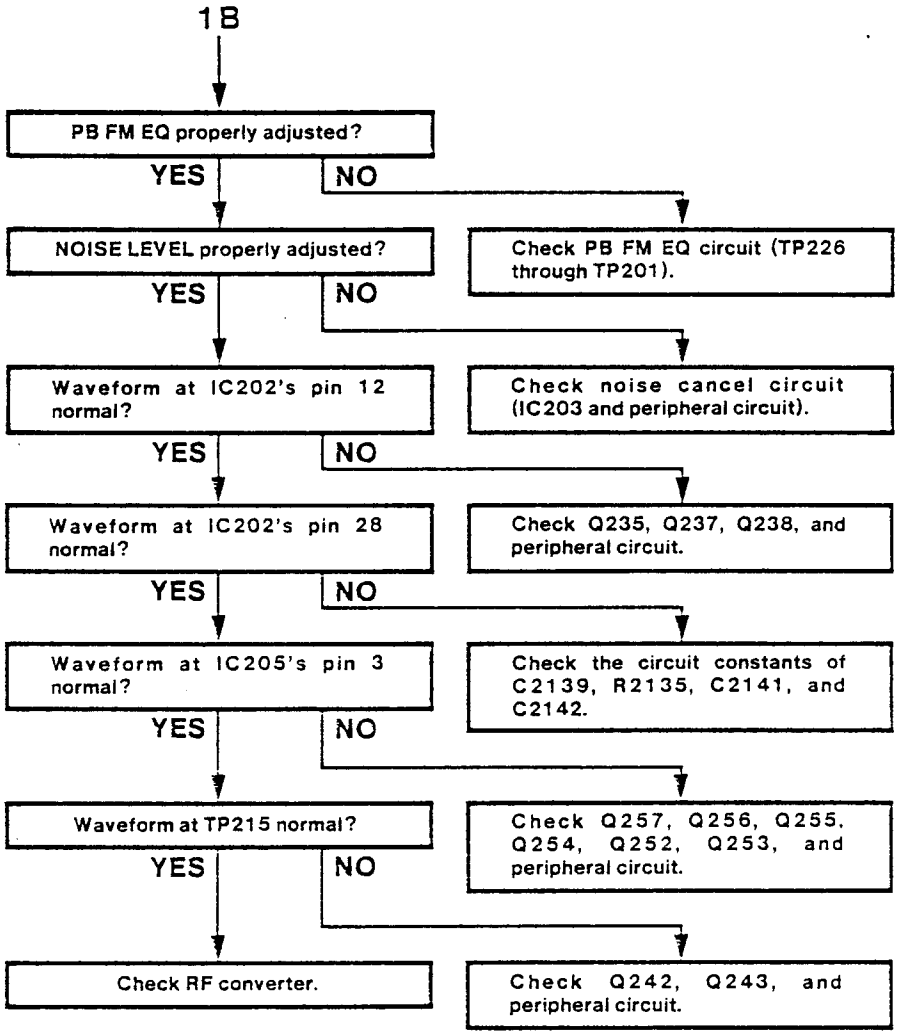
STEP 4. PLAYBACK MODE (LUMINANCE)

1. No picture comes on.



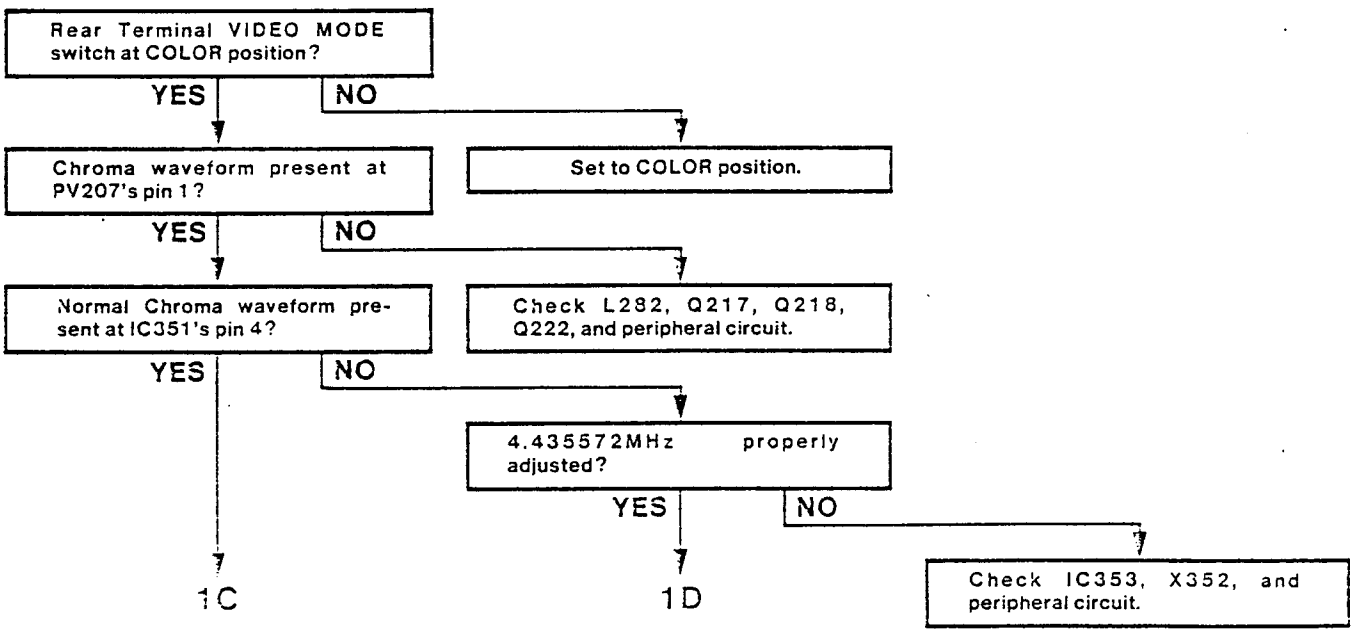
2. Snow, smear, or reverse video appears.

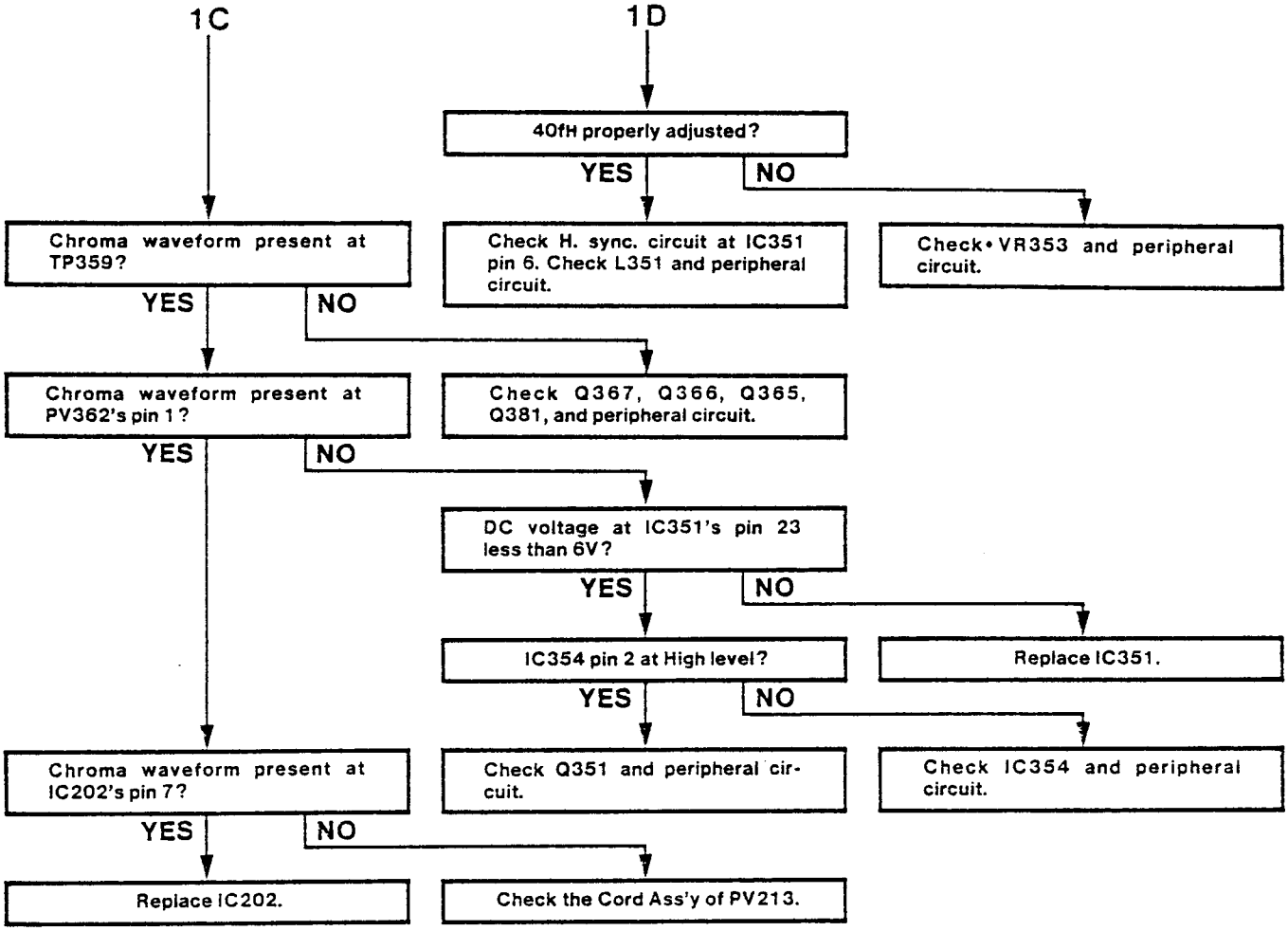




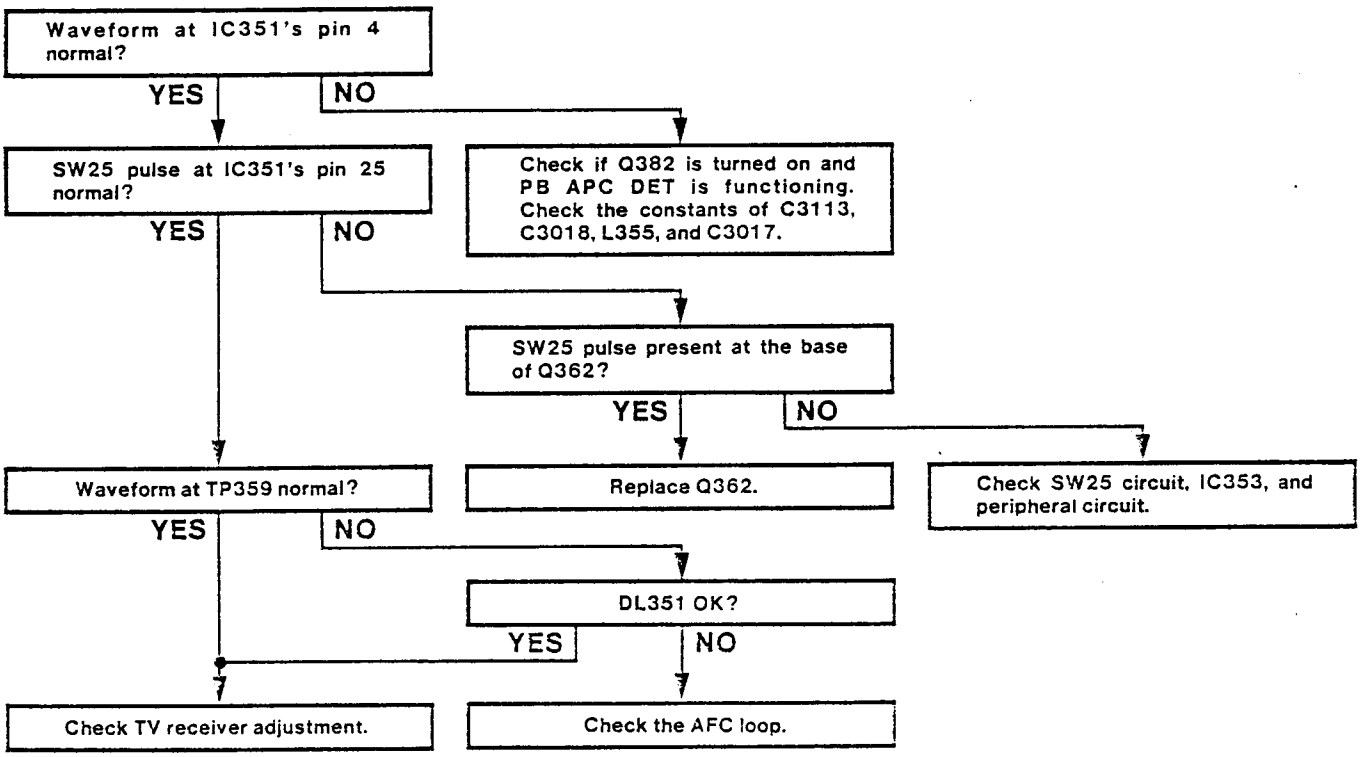
STEP 5. PLAYBACK MODE (CHROMINANCE)

1. Picture completely discolored.



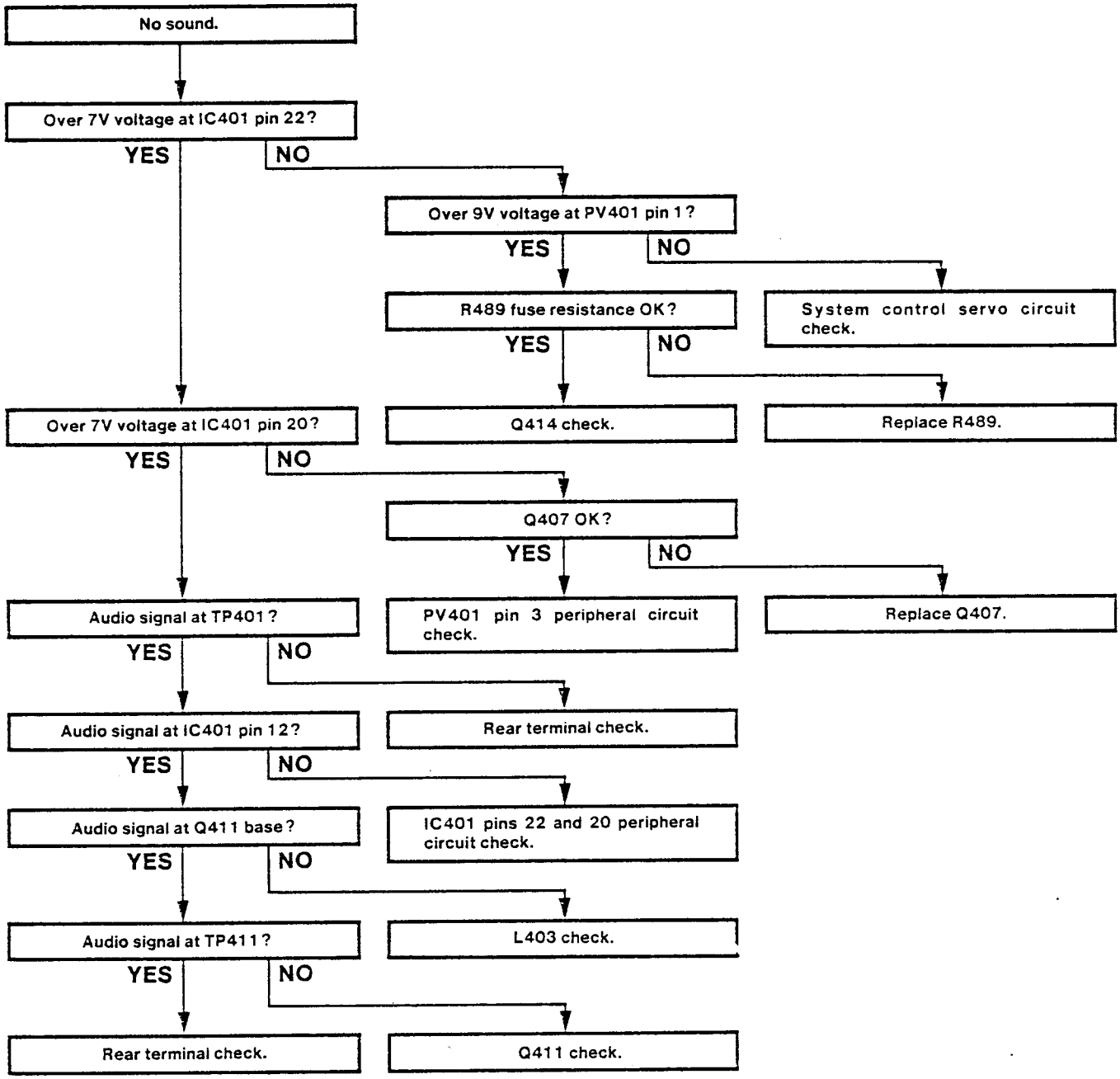


2. Improper color reproduction.

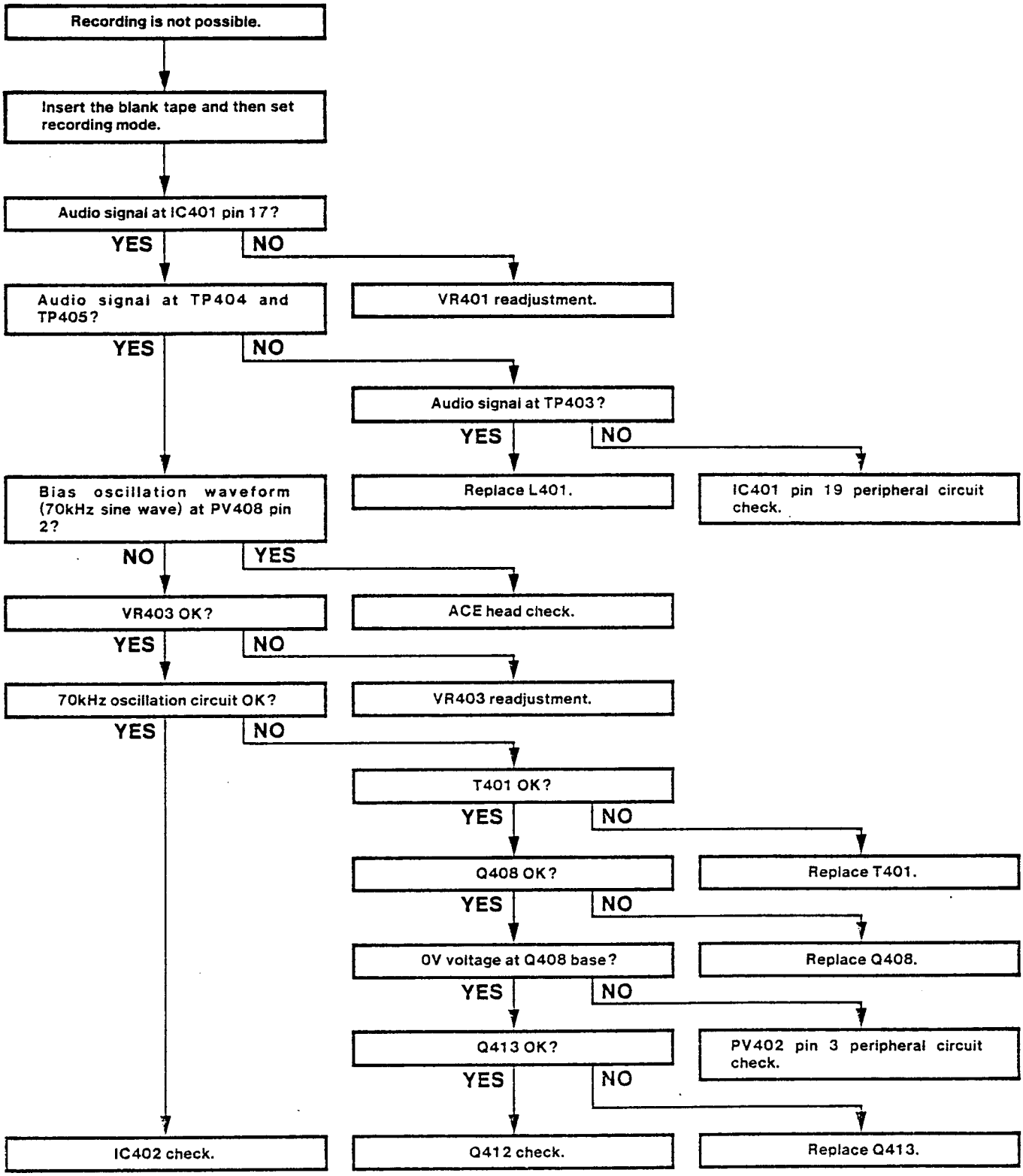


5-2. AUDIO CIRCUIT

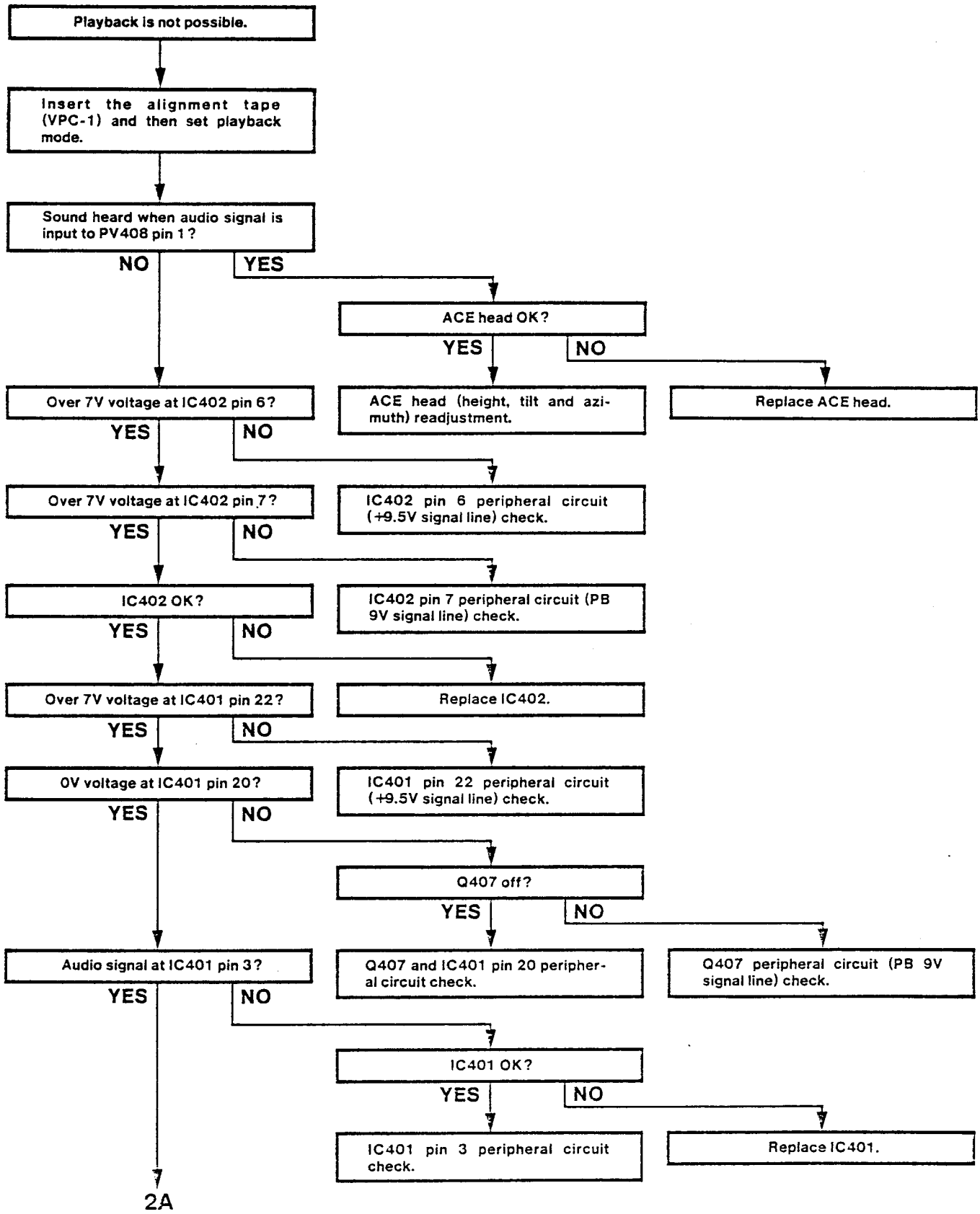
Step 1. STOP MODE (E-E MODE)

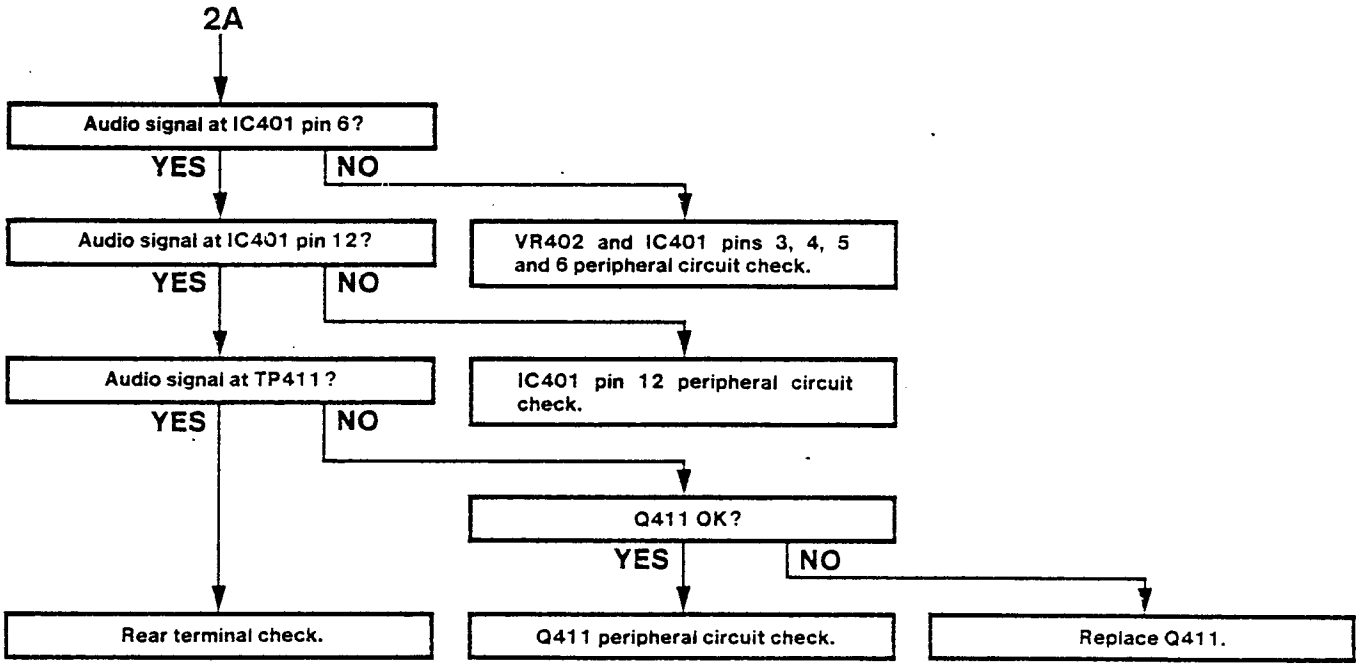


Step 2. RECORDING MODE



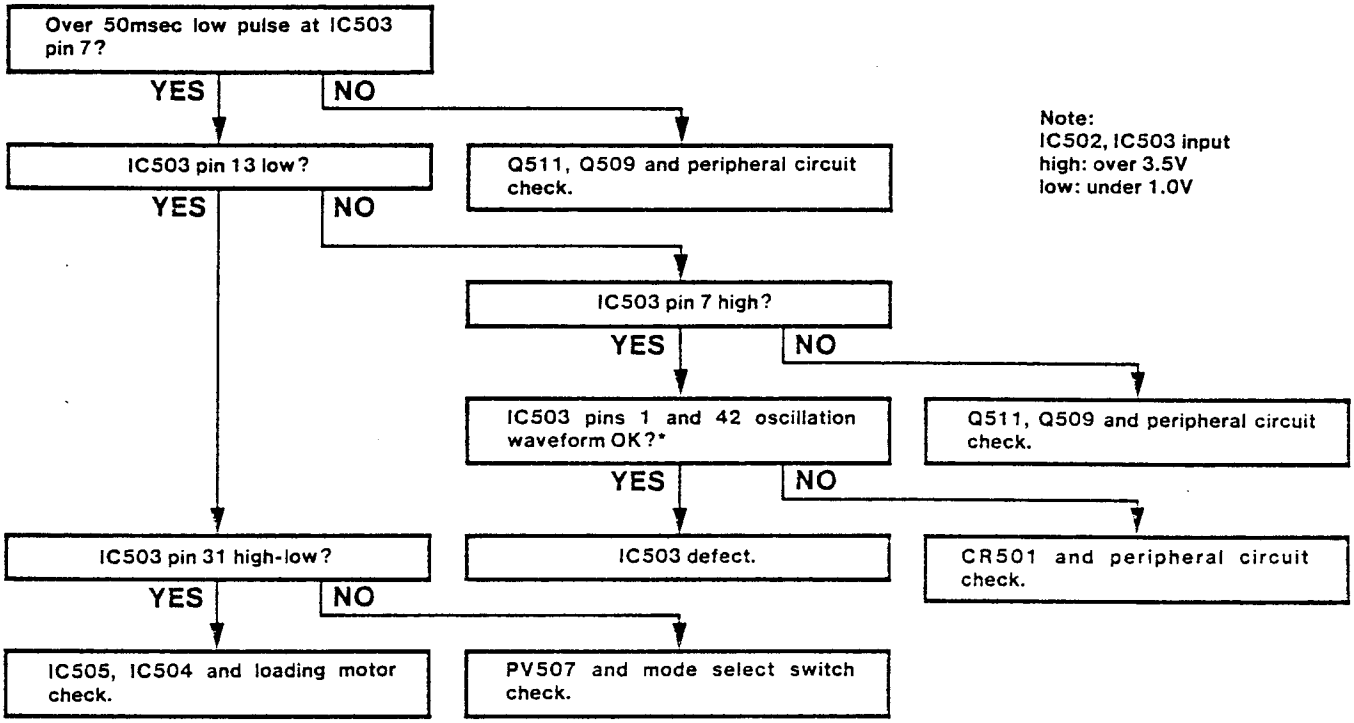
Step 3. PLAYBACK MODE




2A
Audio signal at IC401 pin 6?
YES
NO
Audio signal at IC401 pin 12?
VR402 and IC401 pins 3, 4, 5 and 6 peripheral circuit check.
YES
NO
Audio signal at TP411?
IC401 pin 12 peripheral circuit check.
YES
NO
Q411 OK?
YES
NO
Rear terminal check.
Q411 peripheral circuit check.
Replace Q411.

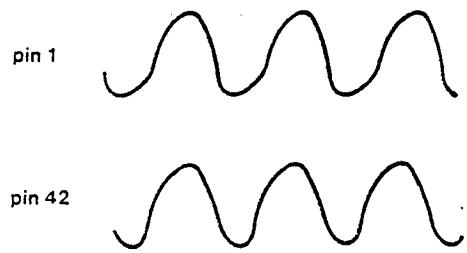
5-3. SYSTEM CONTROL CIRCUIT

Step 1. When power cord is connected to an AC outlet, the unit does not enter the initial condition. (detection of the stop mode is not possible.)



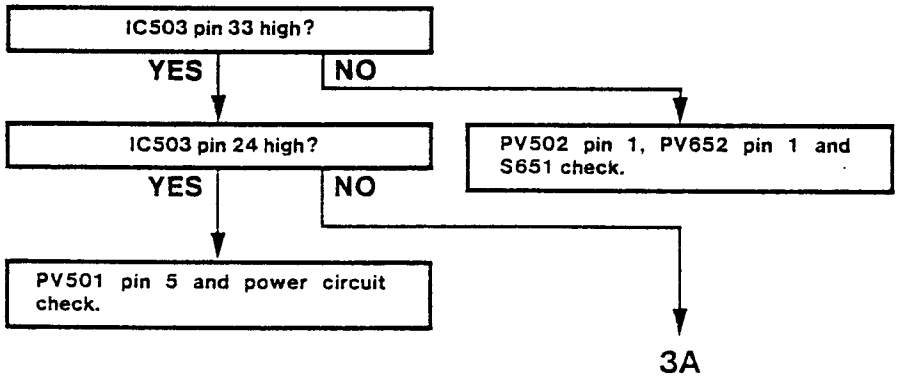
Note:
IC502, IC503 input
high: over 3.5V
low: under 1.0V

* IC503 pins 1 and 42 oscillation waveform

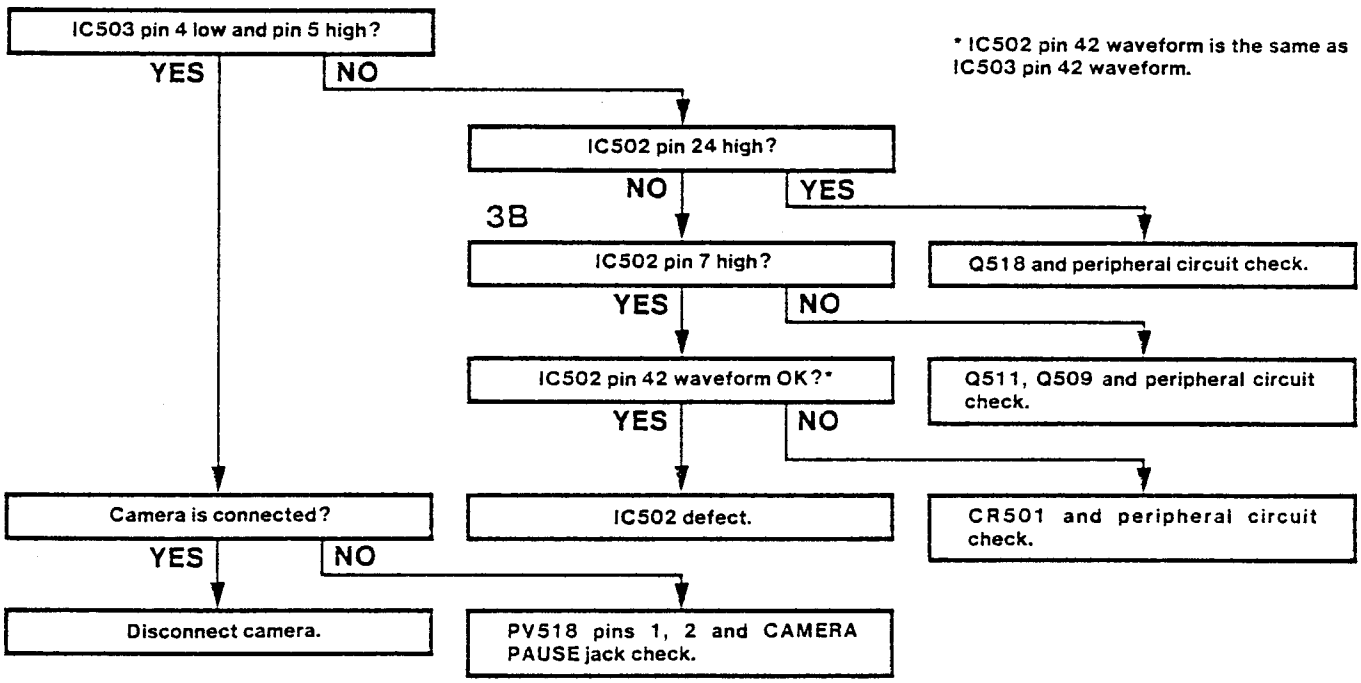


Step 2. Power cannot be switched on.

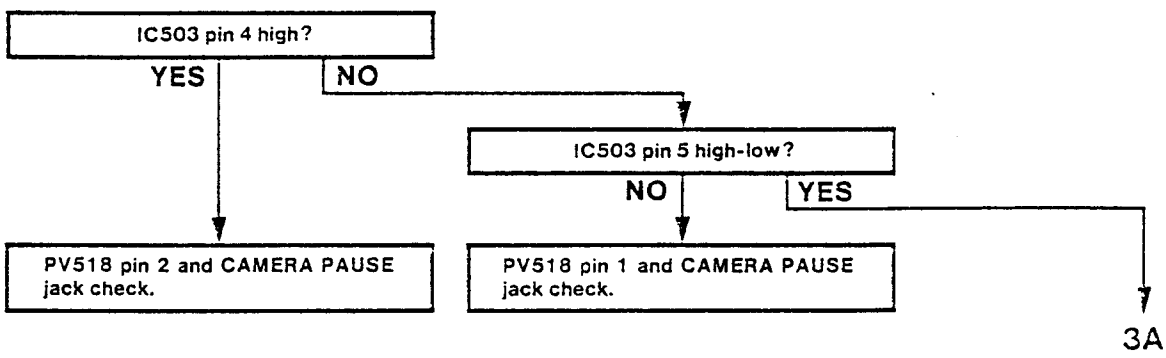
Step 3. Power cannot be switched off.



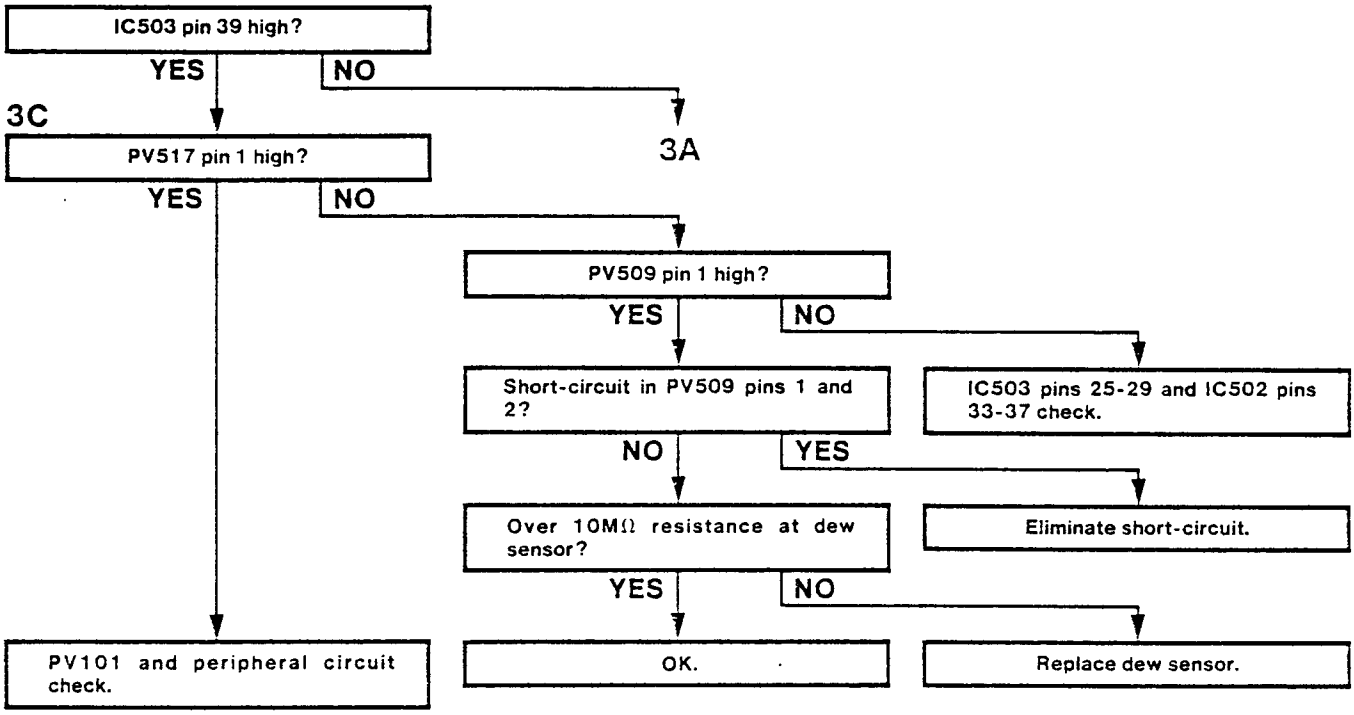
Step 4. Pause mode cannot be released.



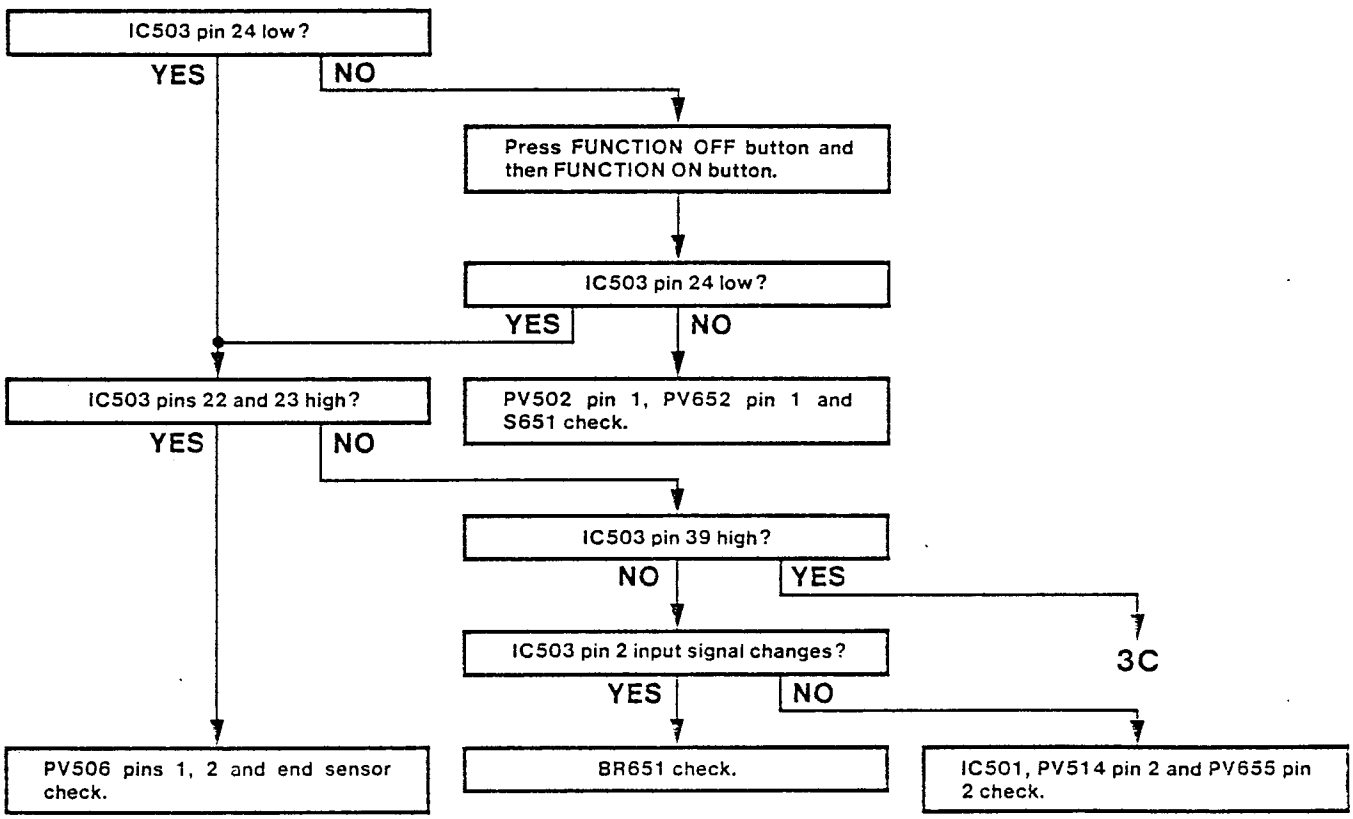
Step 5. Camera pause mode is not possible.



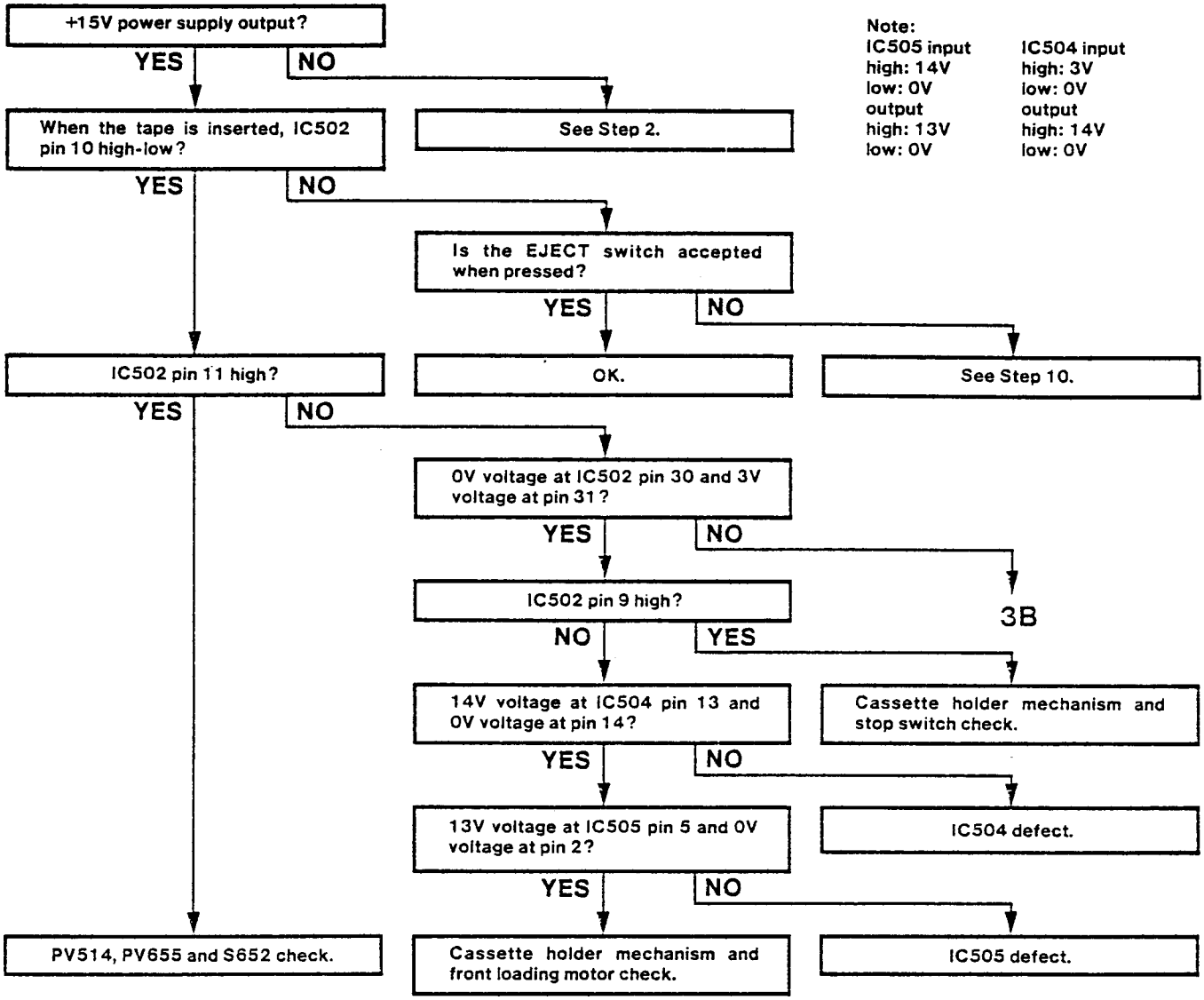
Step 6. Dew LED is blinking.



Step 7. None of the keys operate.



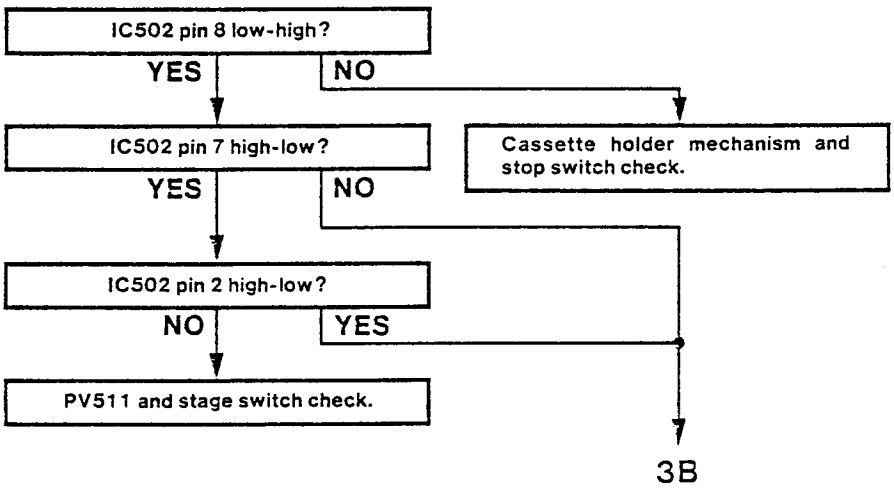
Step 8. Front loading is not possible.



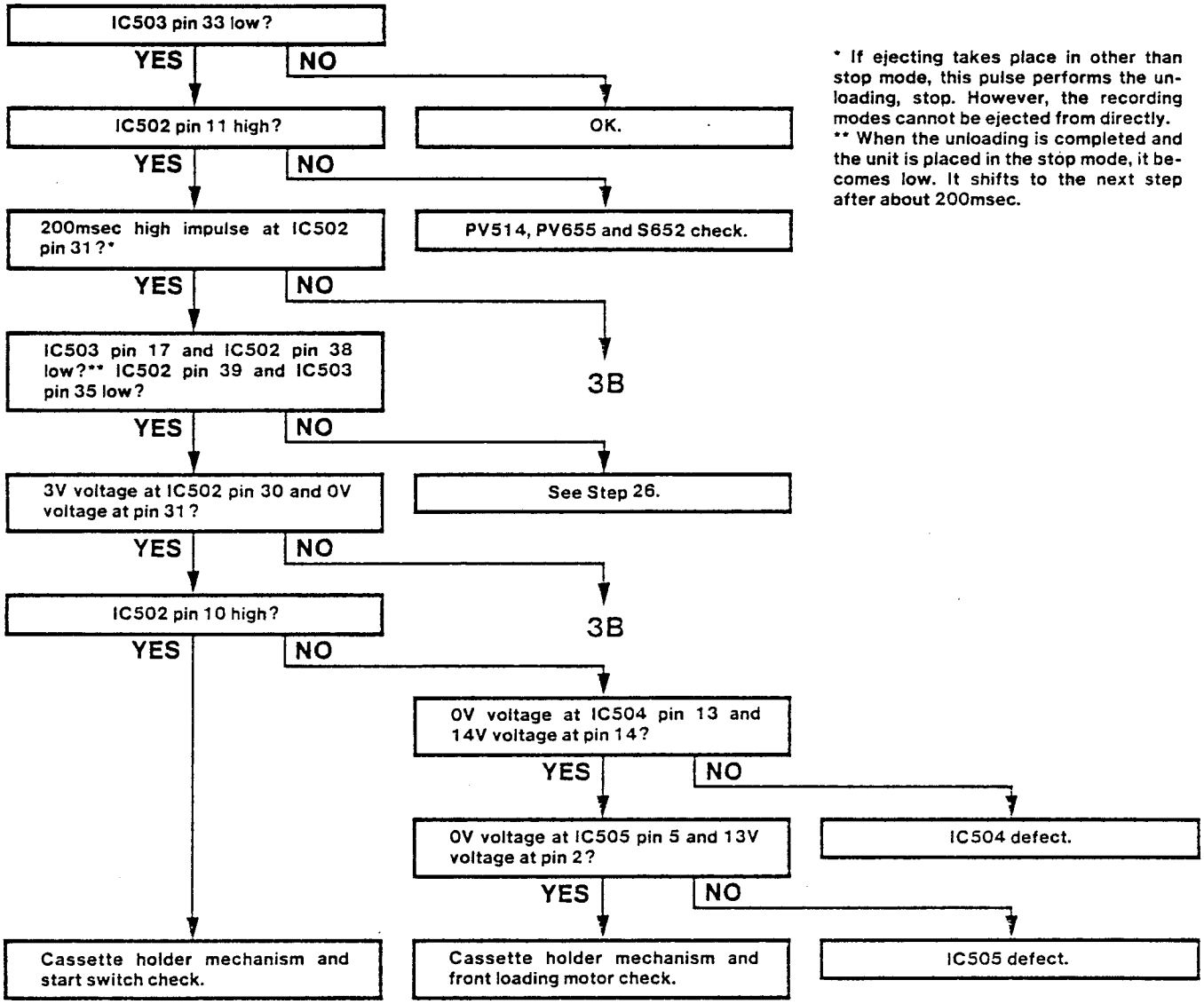
Note:

IC505 input	IC504 input
high: 14V	high: 3V
low: 0V	low: 0V
output	output
high: 13V	high: 14V
low: 0V	low: 0V

Step 9. After front loading, the cassette is ejected immediately.

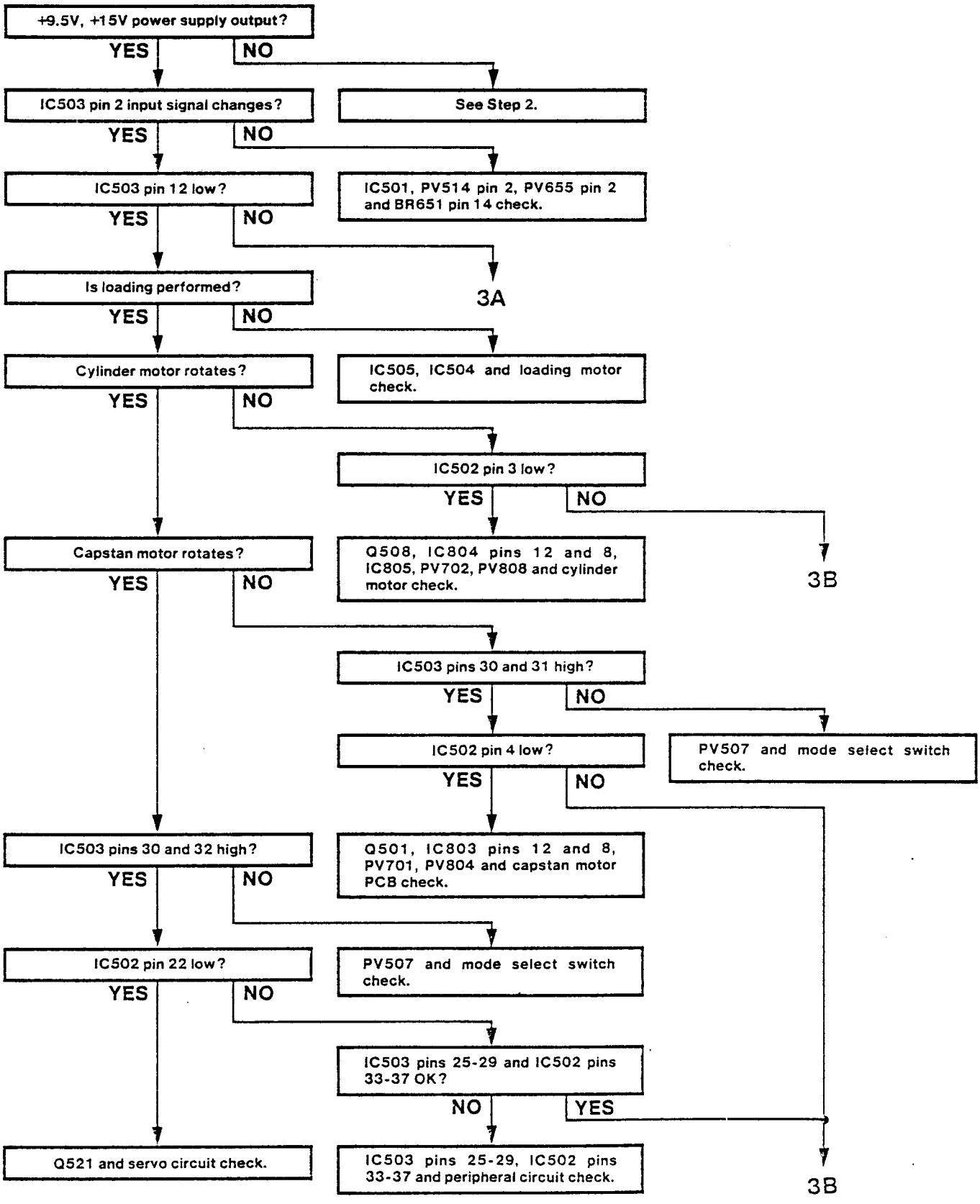


Step 10. Eject is not possible from stop mode.

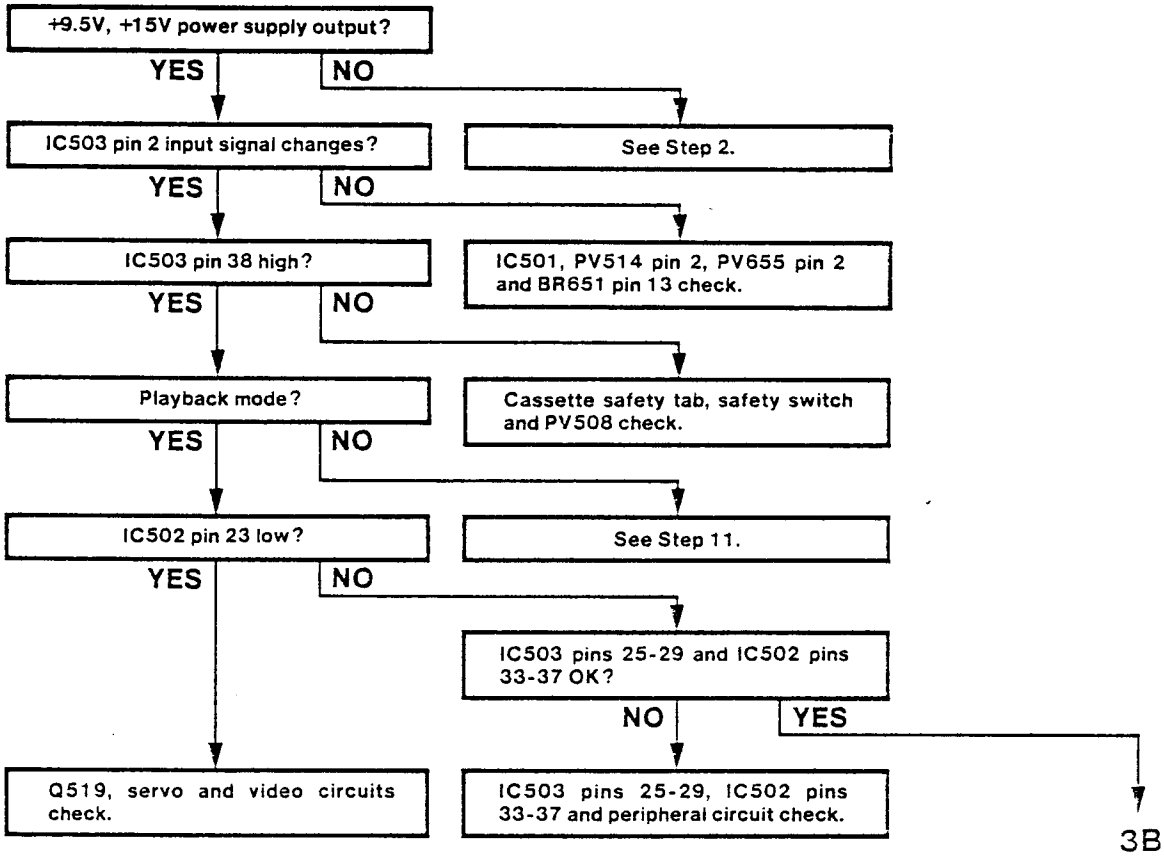


* If ejecting takes place in other than stop mode, this pulse performs the unloading, stop. However, the recording modes cannot be ejected from directly.
** When the unloading is completed and the unit is placed in the stop mode, it becomes low. It shifts to the next step after about 200msec.

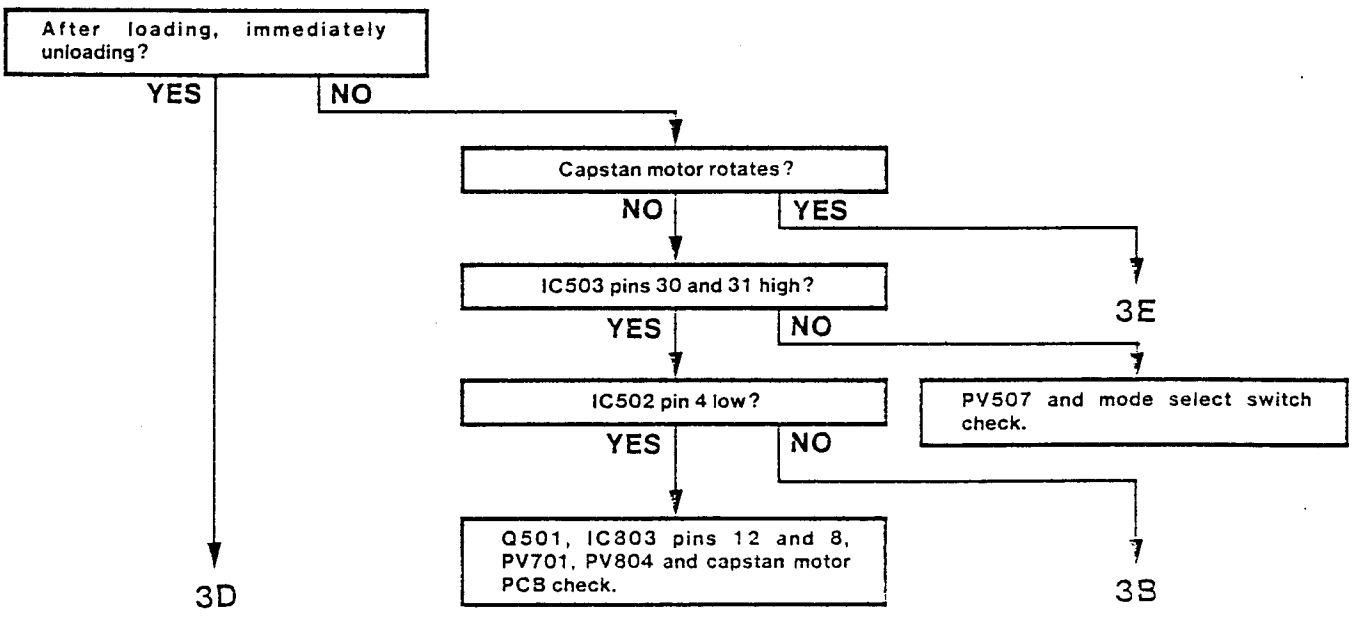
Step 11. Playback is not possible.

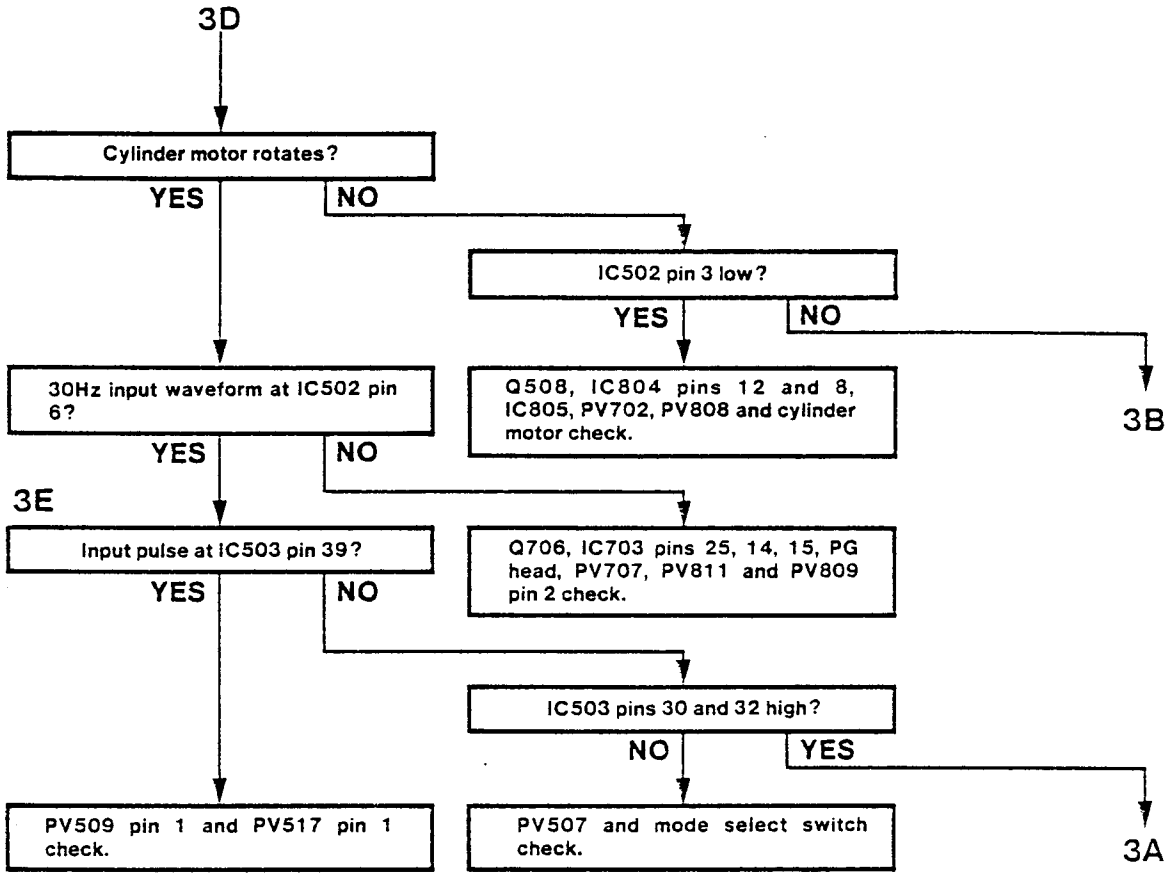


Step 12. Recording is not possible.

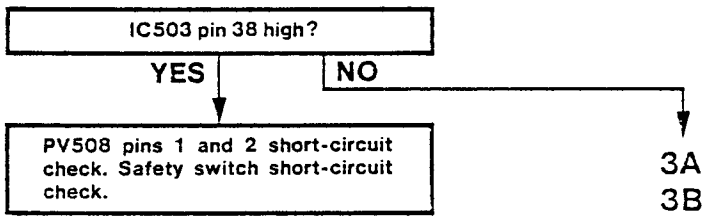


Step 13. Loading is performed but then unloading follows.

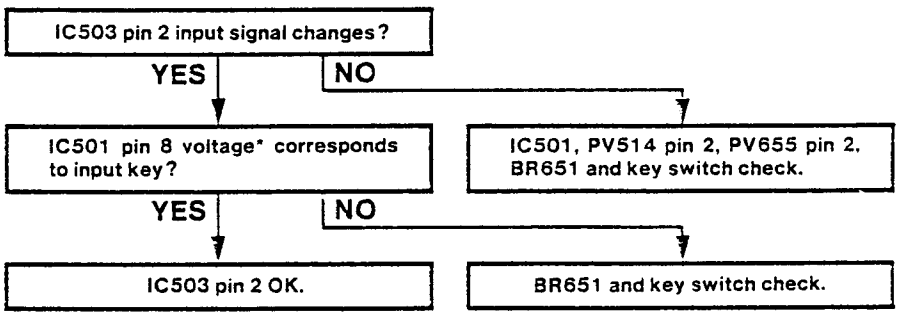




Step 14. Recording is possible when using a cassette which has no safety tab.



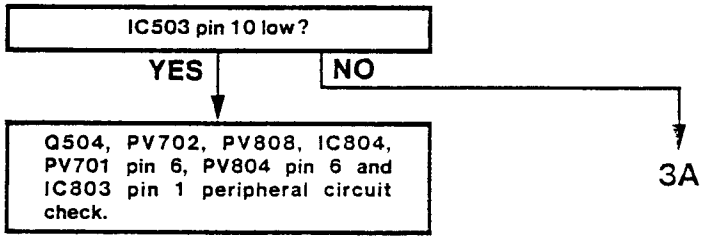
Key input should be performed before checking the items below.



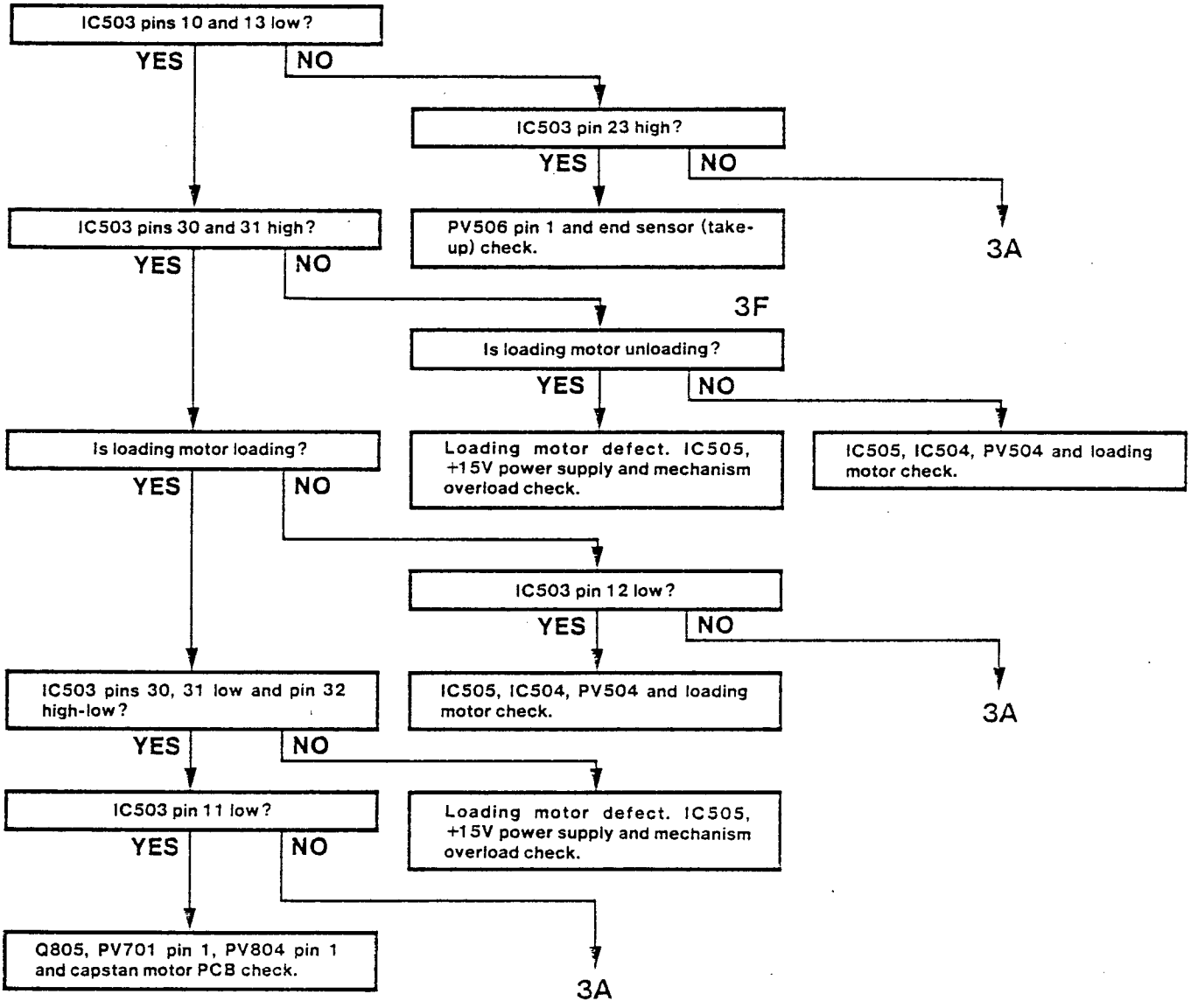
* IC 501 pin 8 voltage

Mode	Voltage (V)
Playback	9.18 ~ 9.24
Recording	9.00 ~ 9.07
Fast forward/cue	7.80 ~ 7.89
Rewind/review	7.64 ~ 7.73
Stop	7.47 ~ 7.58
Speed	7.31 ~ 7.42
Eject	7.15 ~ 7.26
Pause	6.99 ~ 7.09

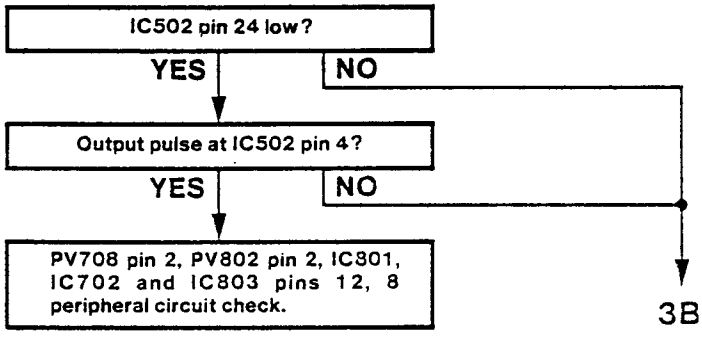
Step 15. Switching from playback to cue is not possible.



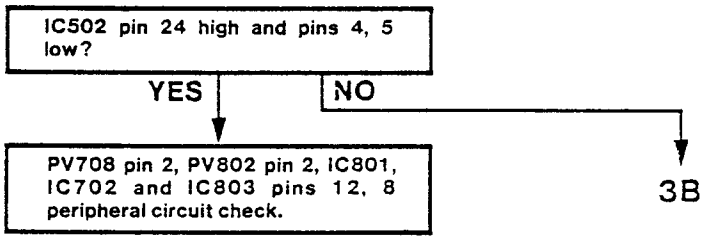
Step 16. Switching from playback to review is not possible.



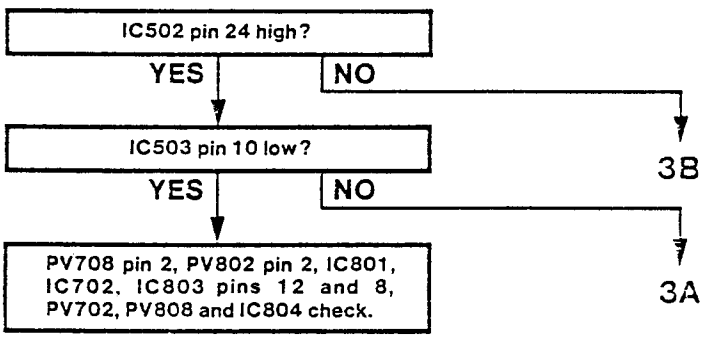
Step 17. Switching from playback to still is not possible.



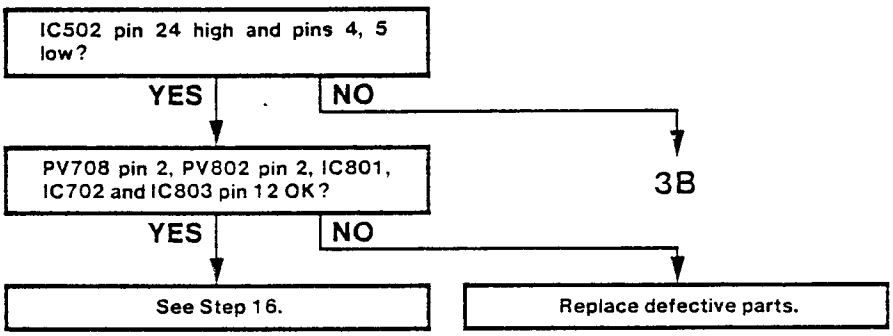
Step 18. Switching from still to playback is not possible.



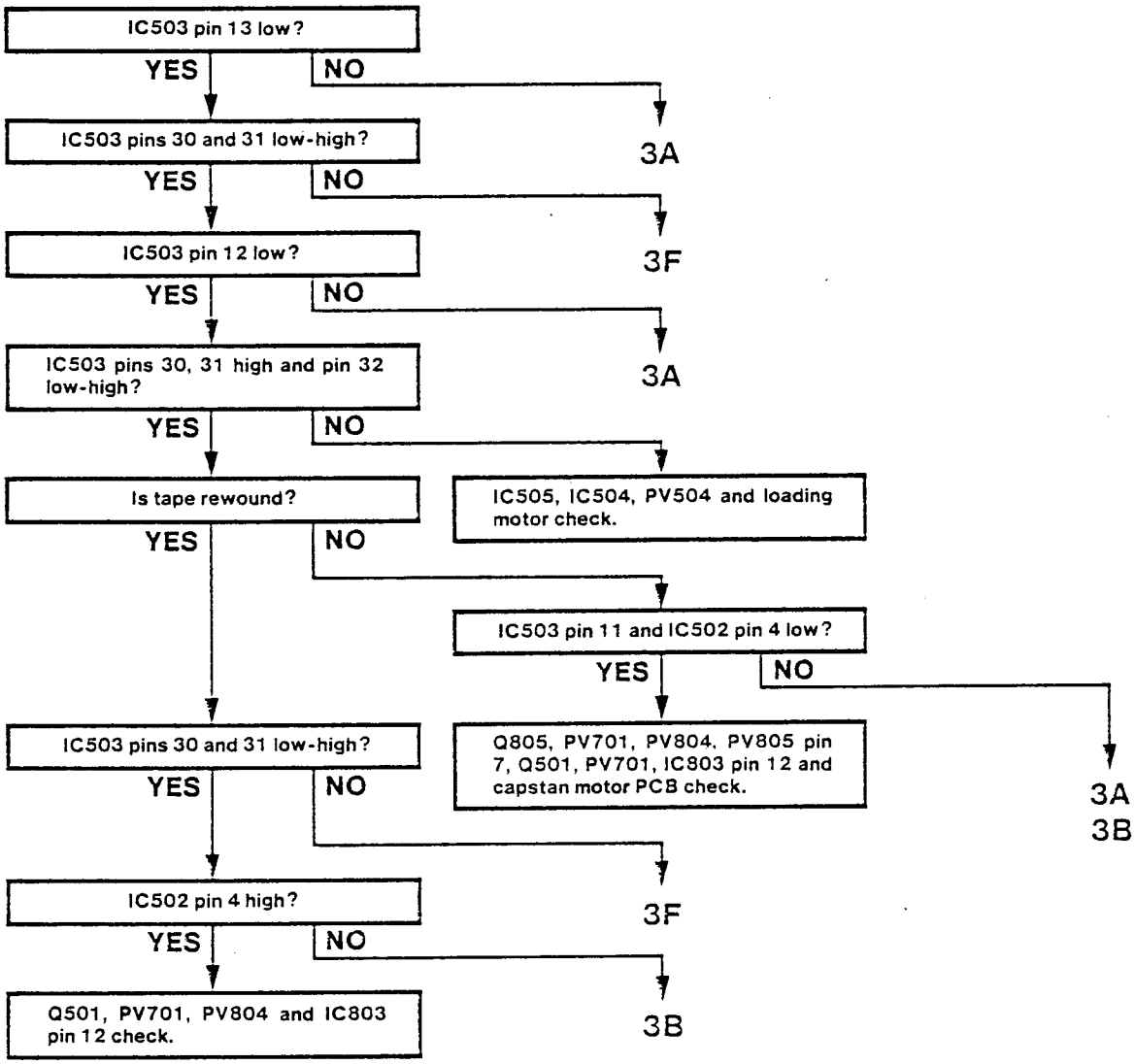
Step 19. Switching from still to cue is not possible.



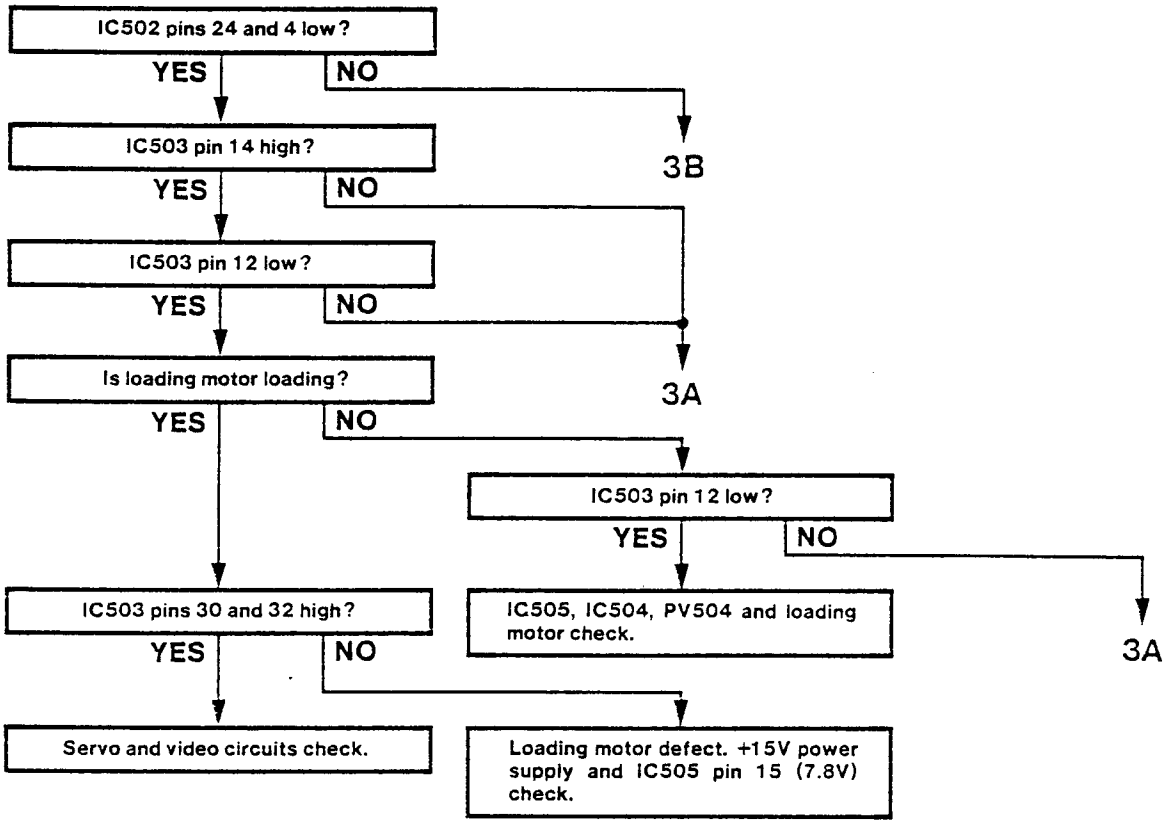
Step 20. Switching from still to review is not possible.



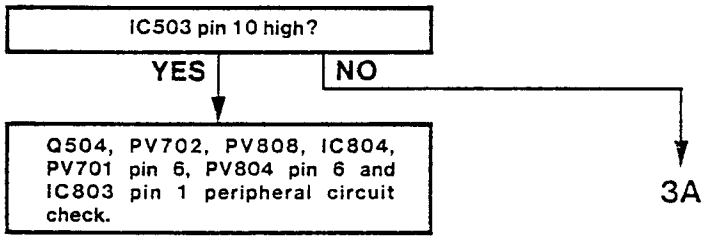
Step 21. Switching from recording to recording pause is not possible.



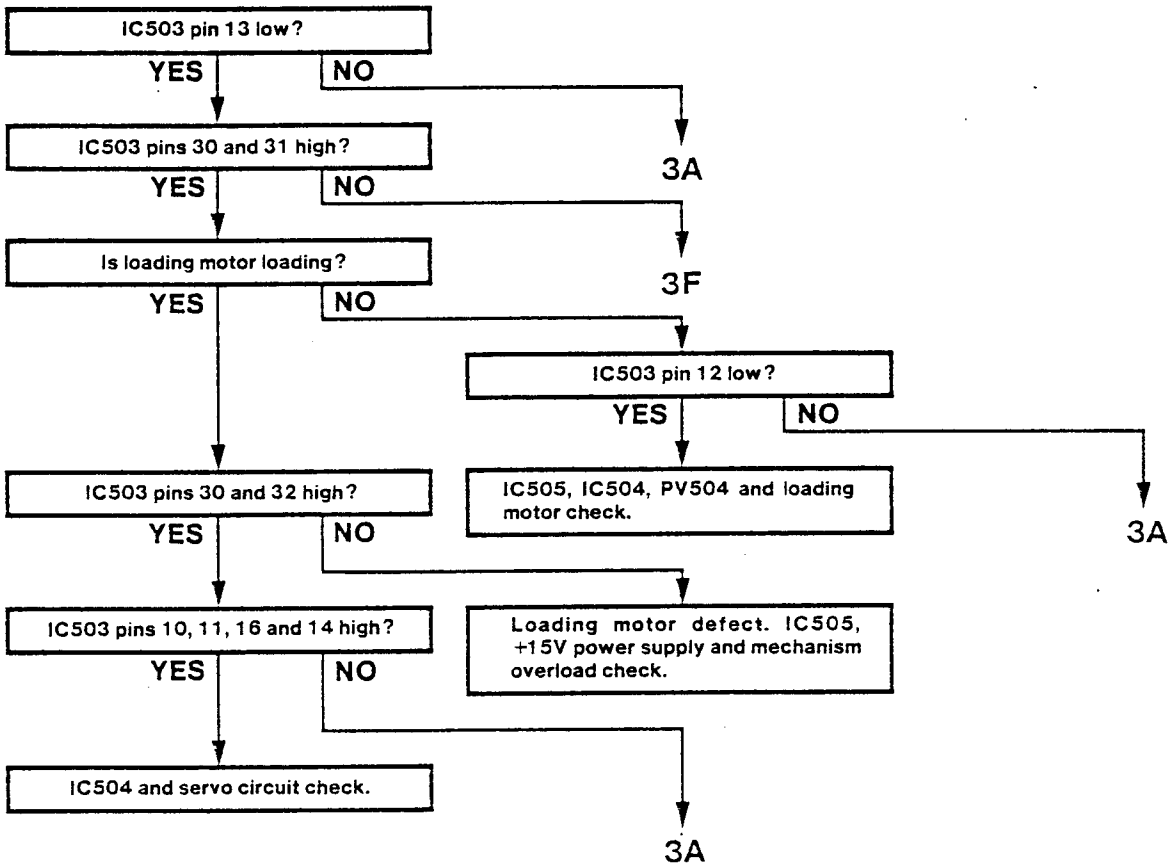
Step 22. Switching from recording pause to recording is not possible.



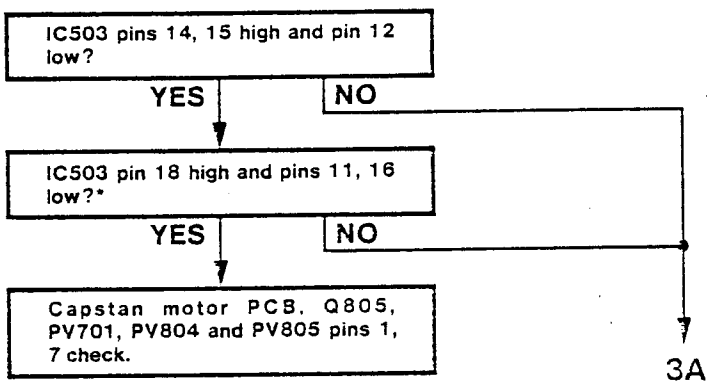
Step 23. Switching from cue to playback is not possible.



Step 24. Switching from review to playback is not possible.

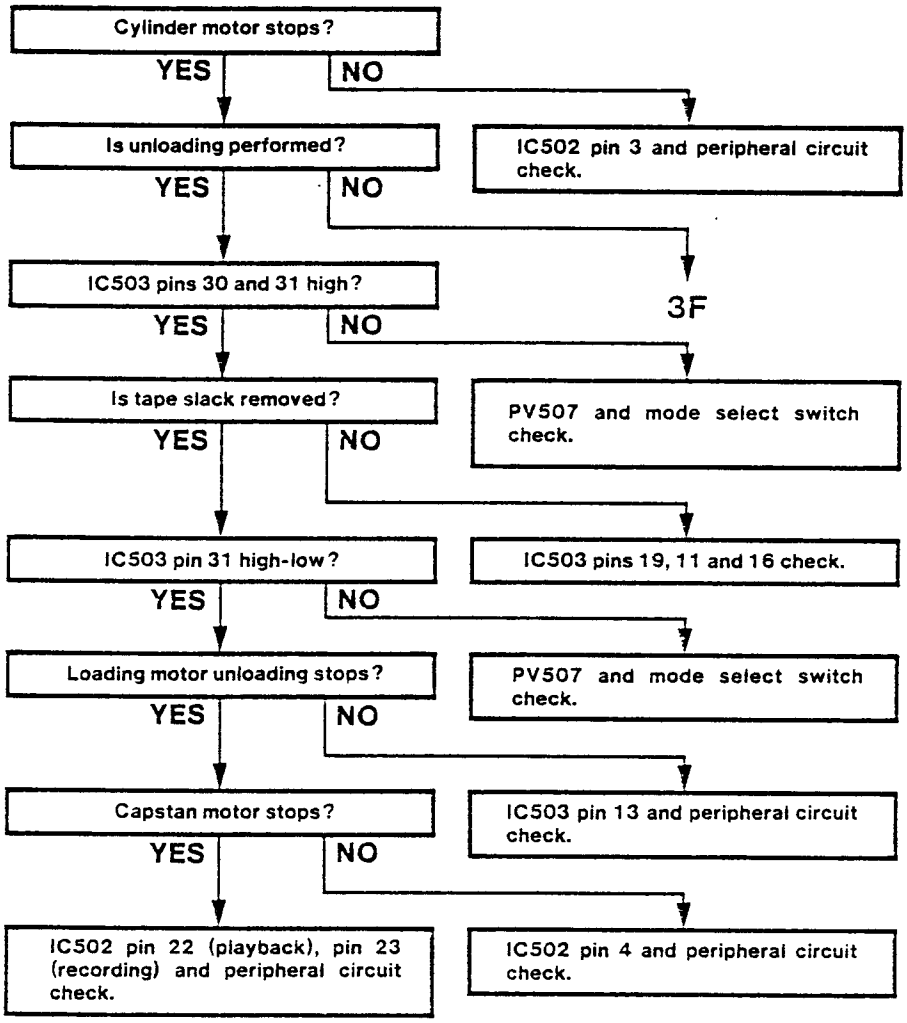


Step 25. Switching from stop to fast forward/rewind is not possible.

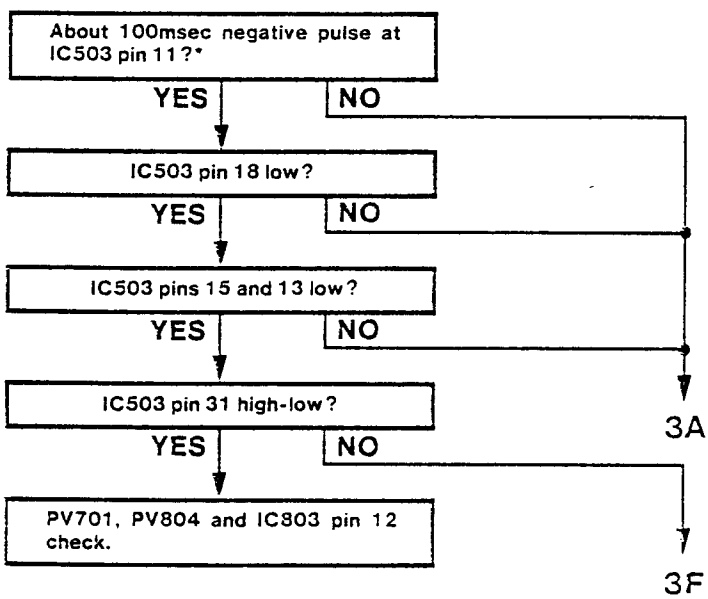


* In case of rewinding, pins 11, 16 high-low.

Step 26. Switching from loading mode to stop is not possible.

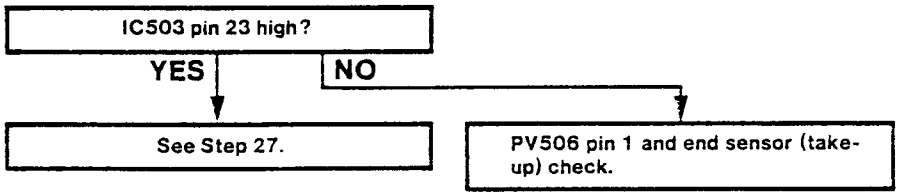


Step 27. Switching from fast forward/rewind to stop is not possible.

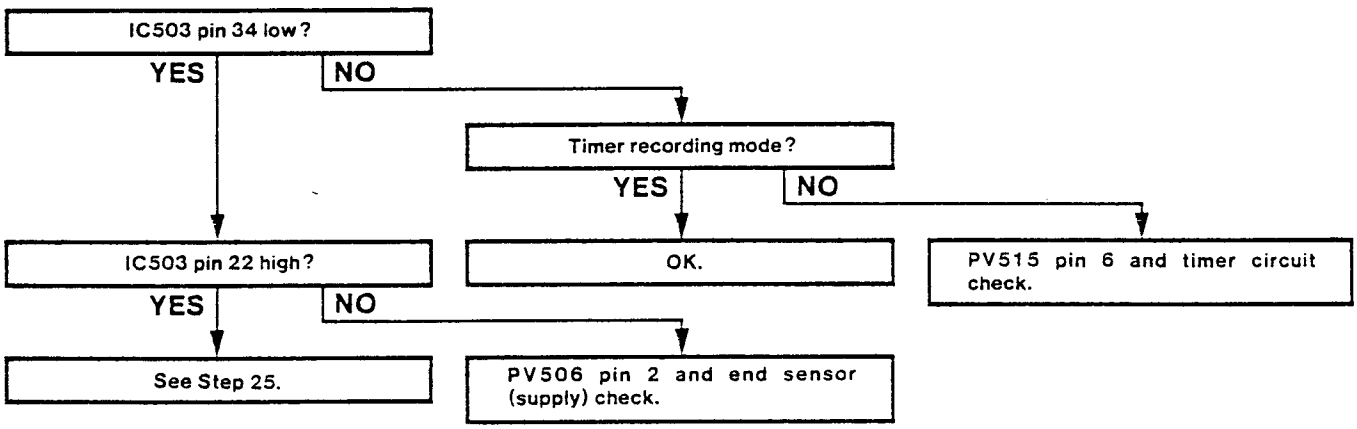


* Only when switching from fast forward to stop. When switching from rewind to stop, IC503 pin 11 becomes low-high.

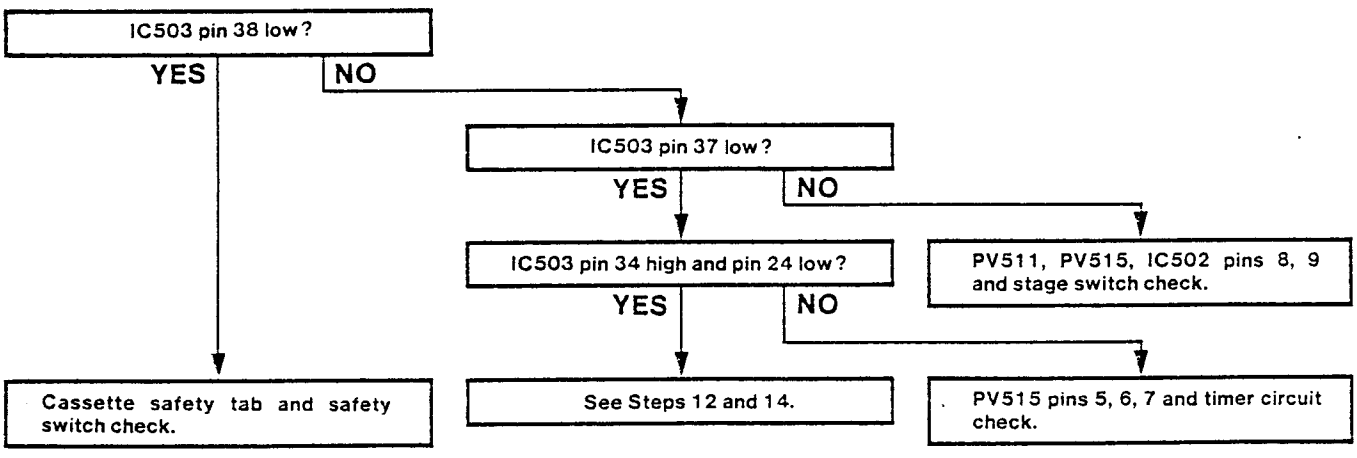
Step 28. Auto stop does not function after rewinding.



Step 29. Auto rewind is not activated.

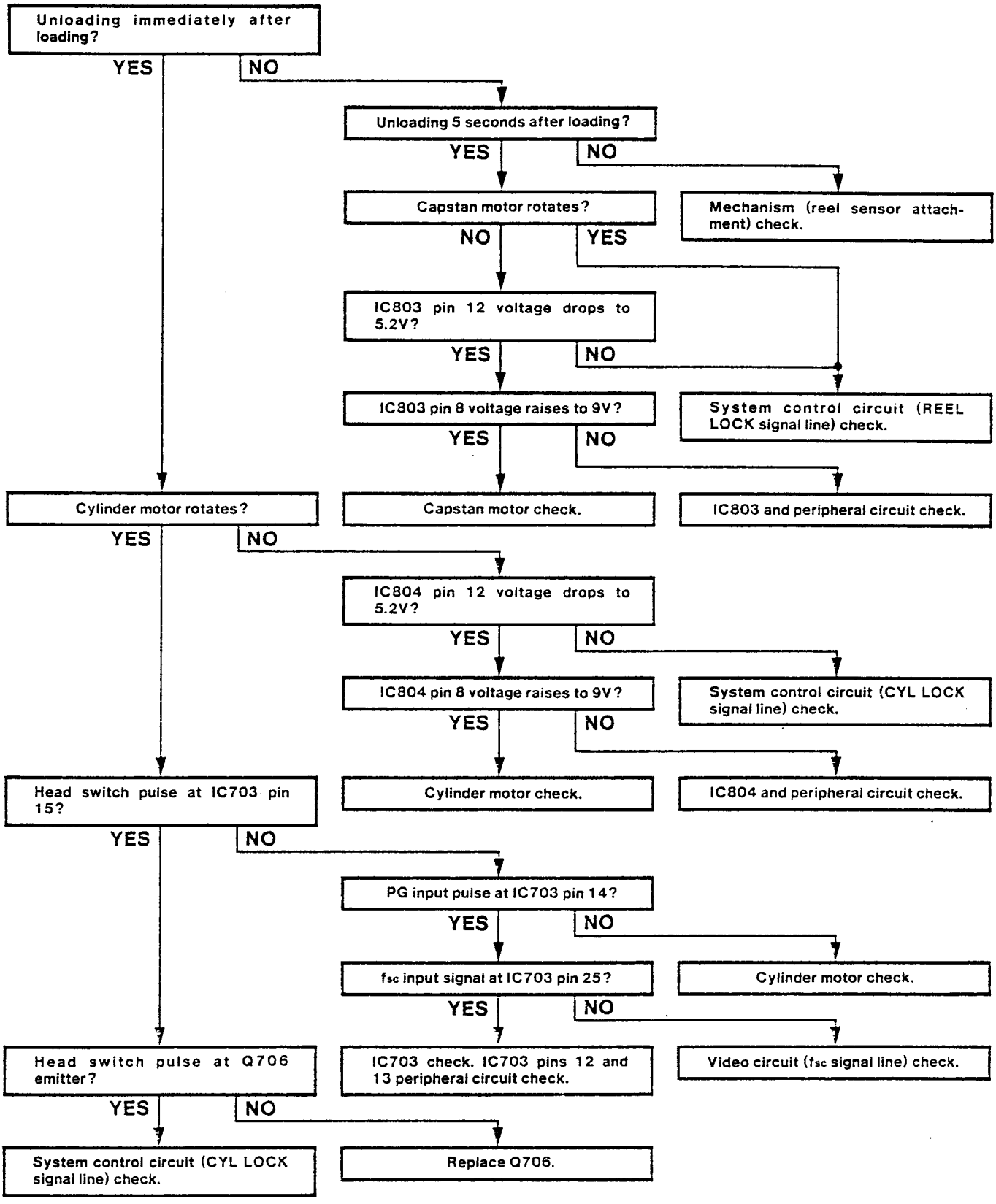


Step 30. Timer recording is not possible.

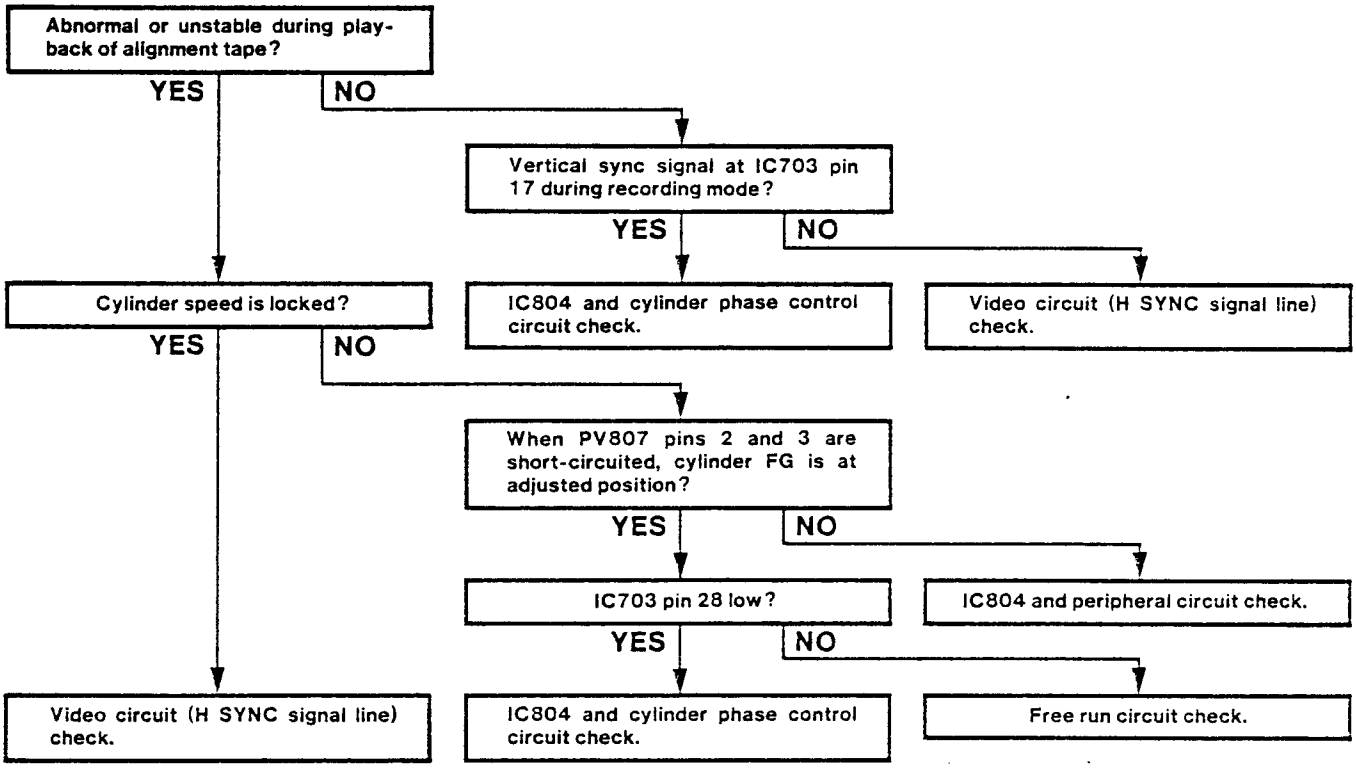


5-4. SERVO CIRCUIT

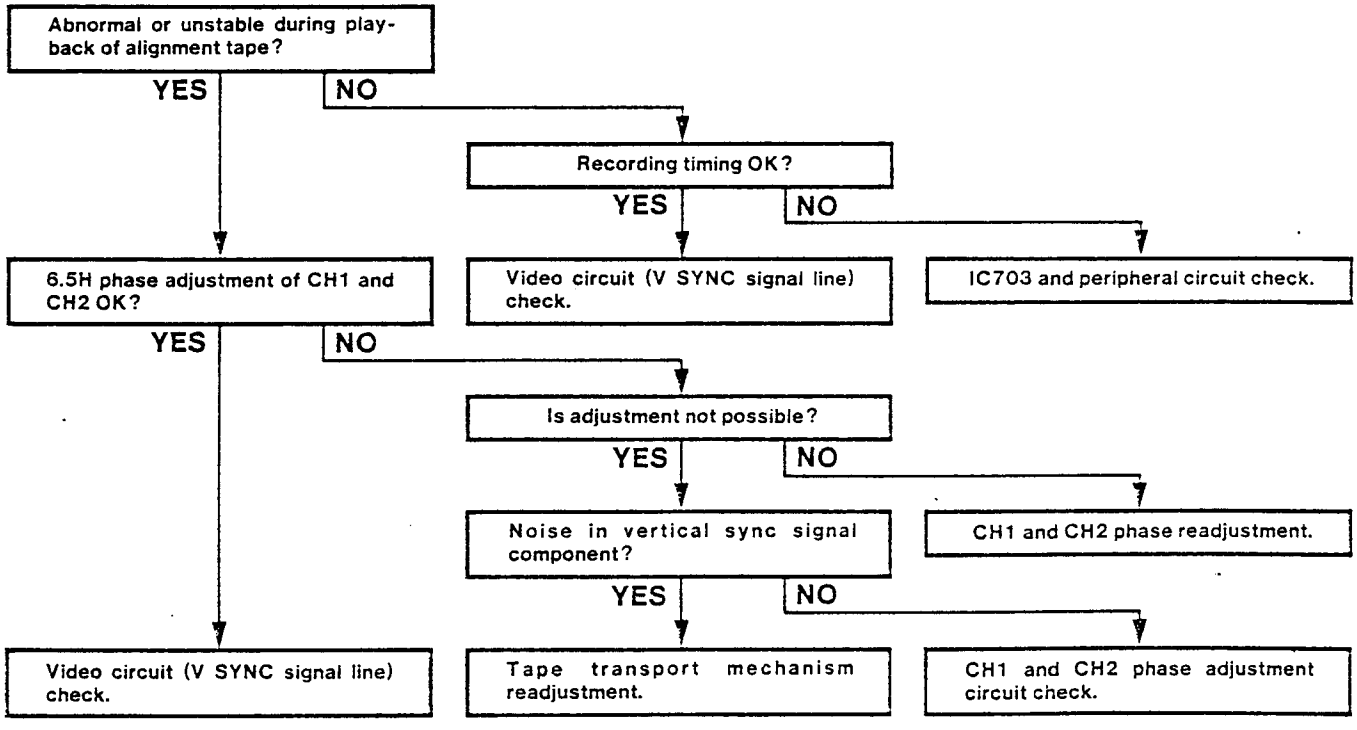
Step 1. Unloading during recording or playback mode.



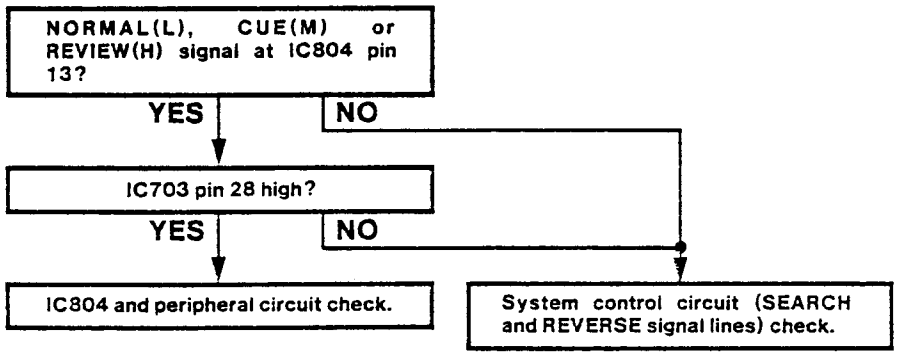
Step 2. Horizontal sync waveform abnormal or unstable during recording or playback mode.



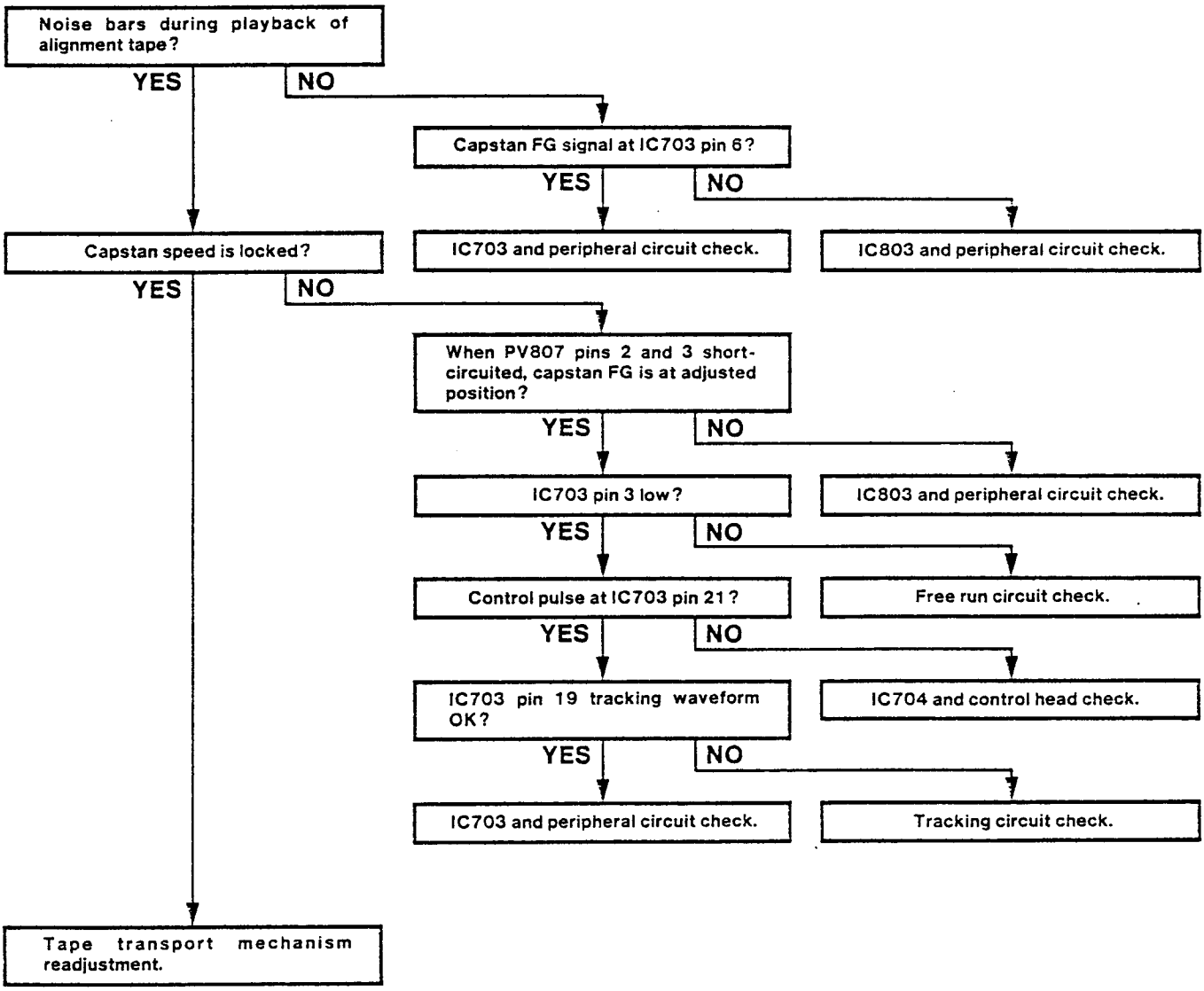
Step 3. Vertical sync waveform abnormal or unstable during recording or playback mode.



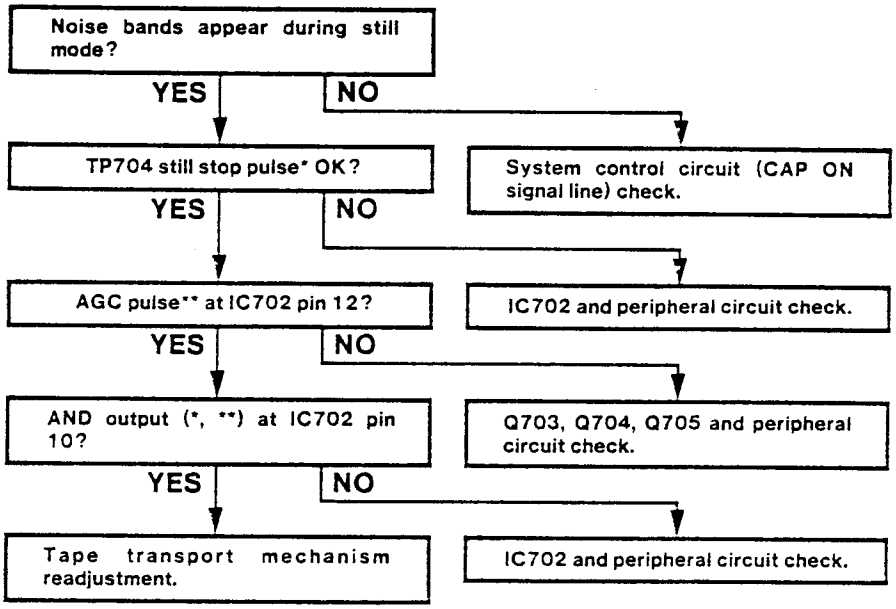
Step 4. Horizontal sync waveform abnormal during cue or review mode.



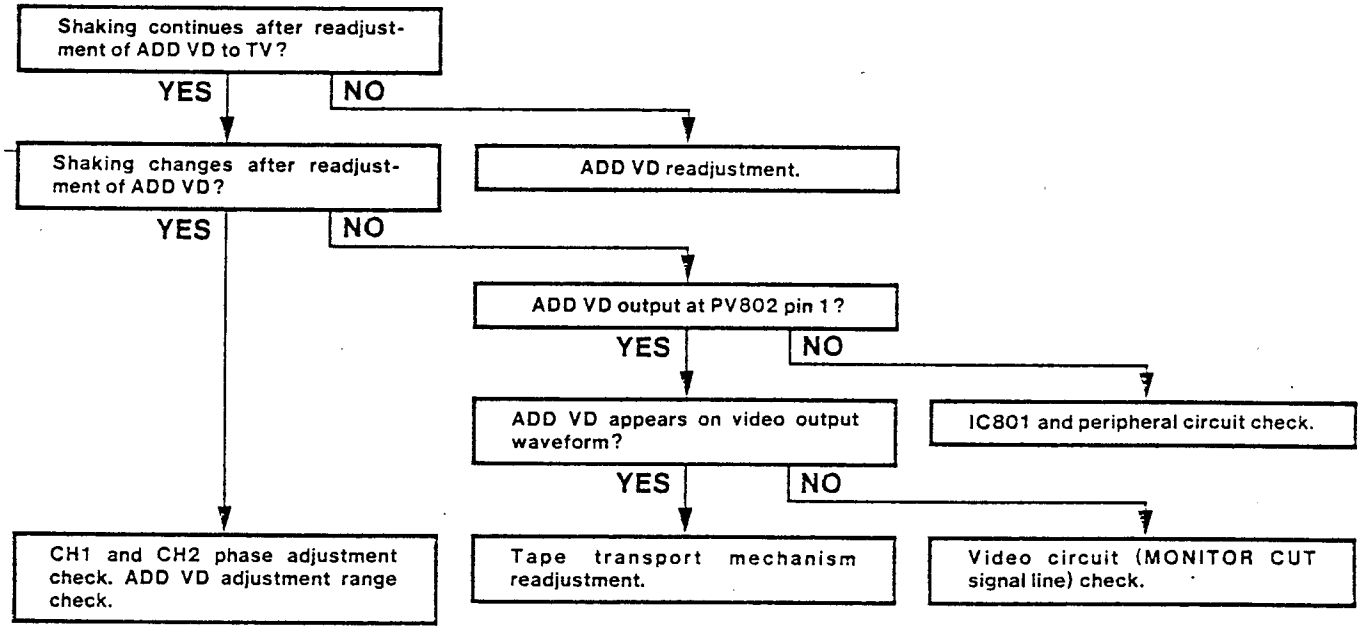
Step 5. Continuous or intermittent noise bars during recording or playback mode.



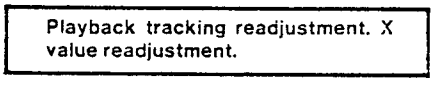
Step 6. Noise bands in the middle of the screen during still mode.



Step 7. Picture shakes during special playback.

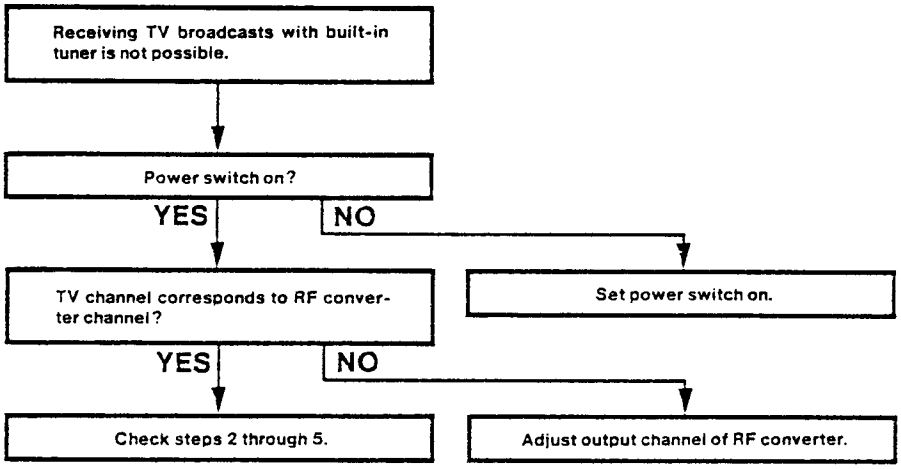


Step 8. No tracking.

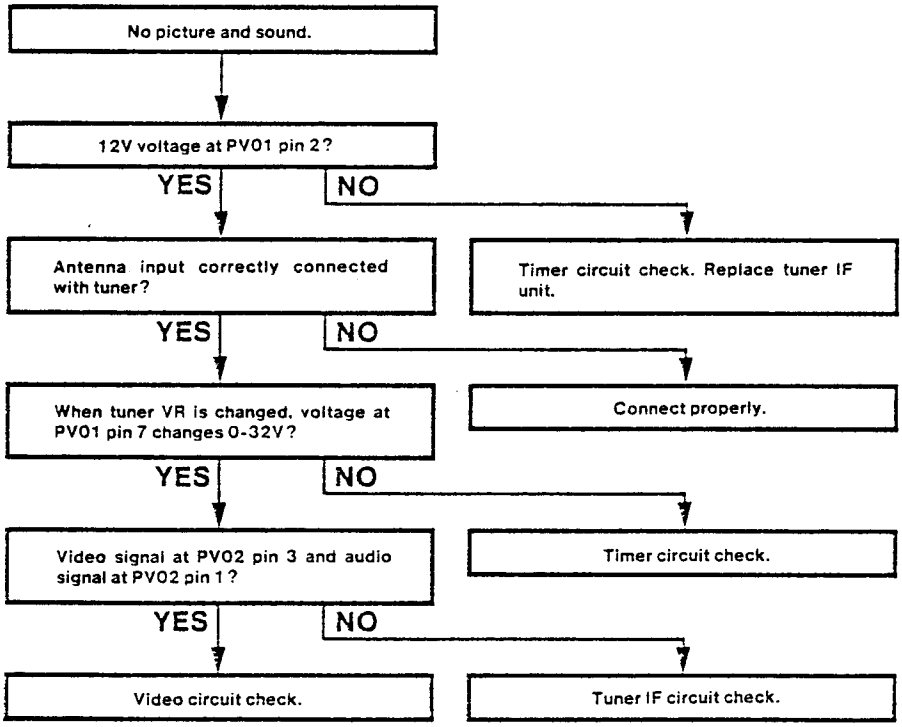


5-5. TUNER CIRCUIT

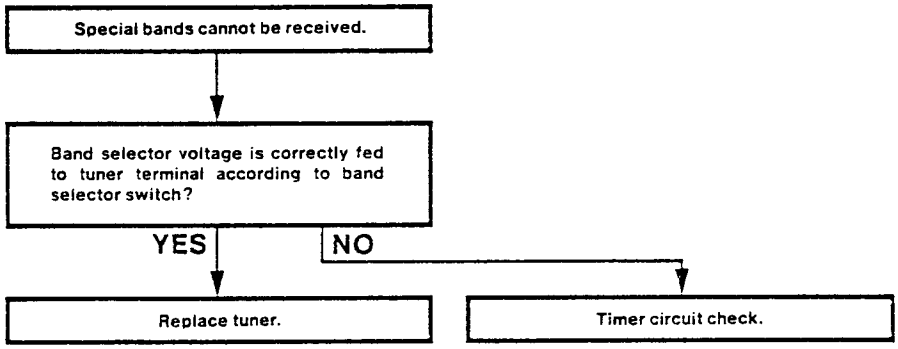
Step 1. Receiving TV broadcasts with built-in tuner is not possible.



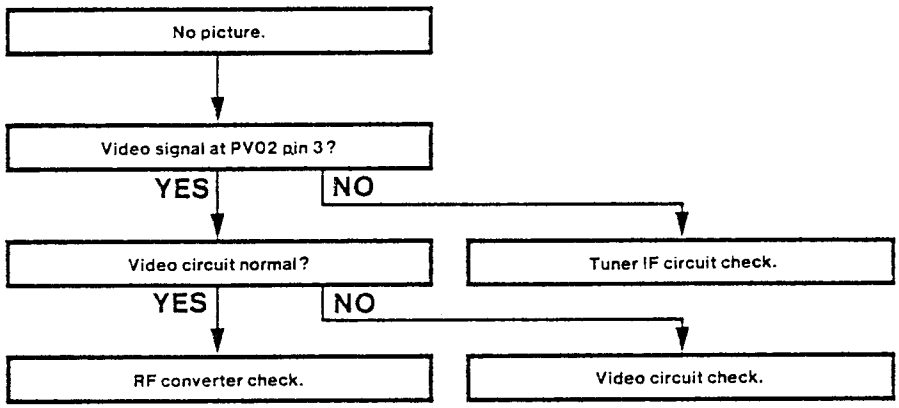
Step 2. No picture and sound.



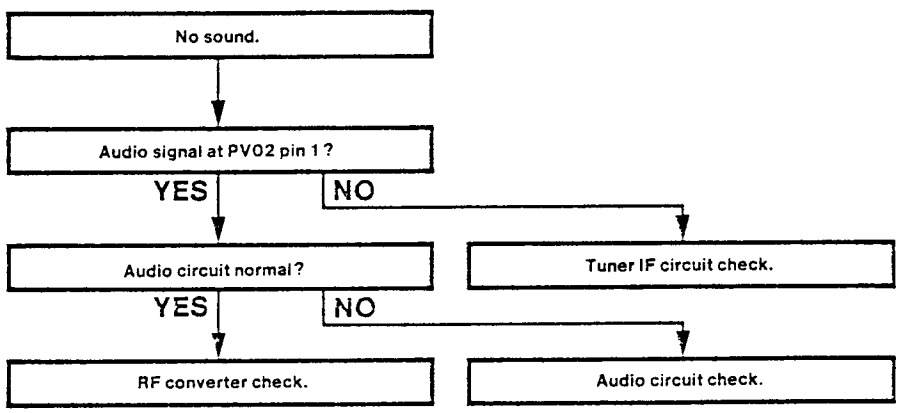
Step 3. Special bands cannot be received.



Step 4. No picture.



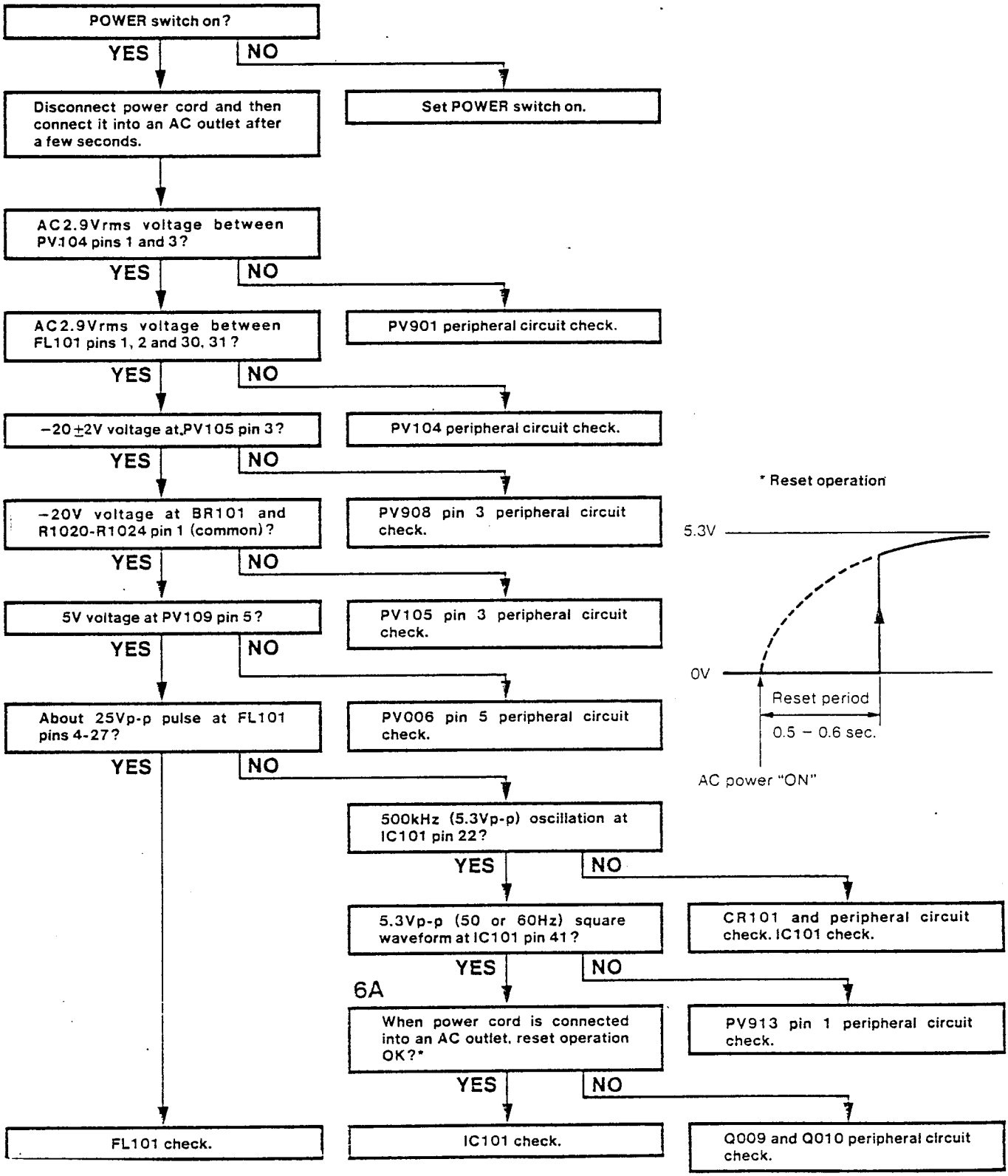
Step 5. No sound.



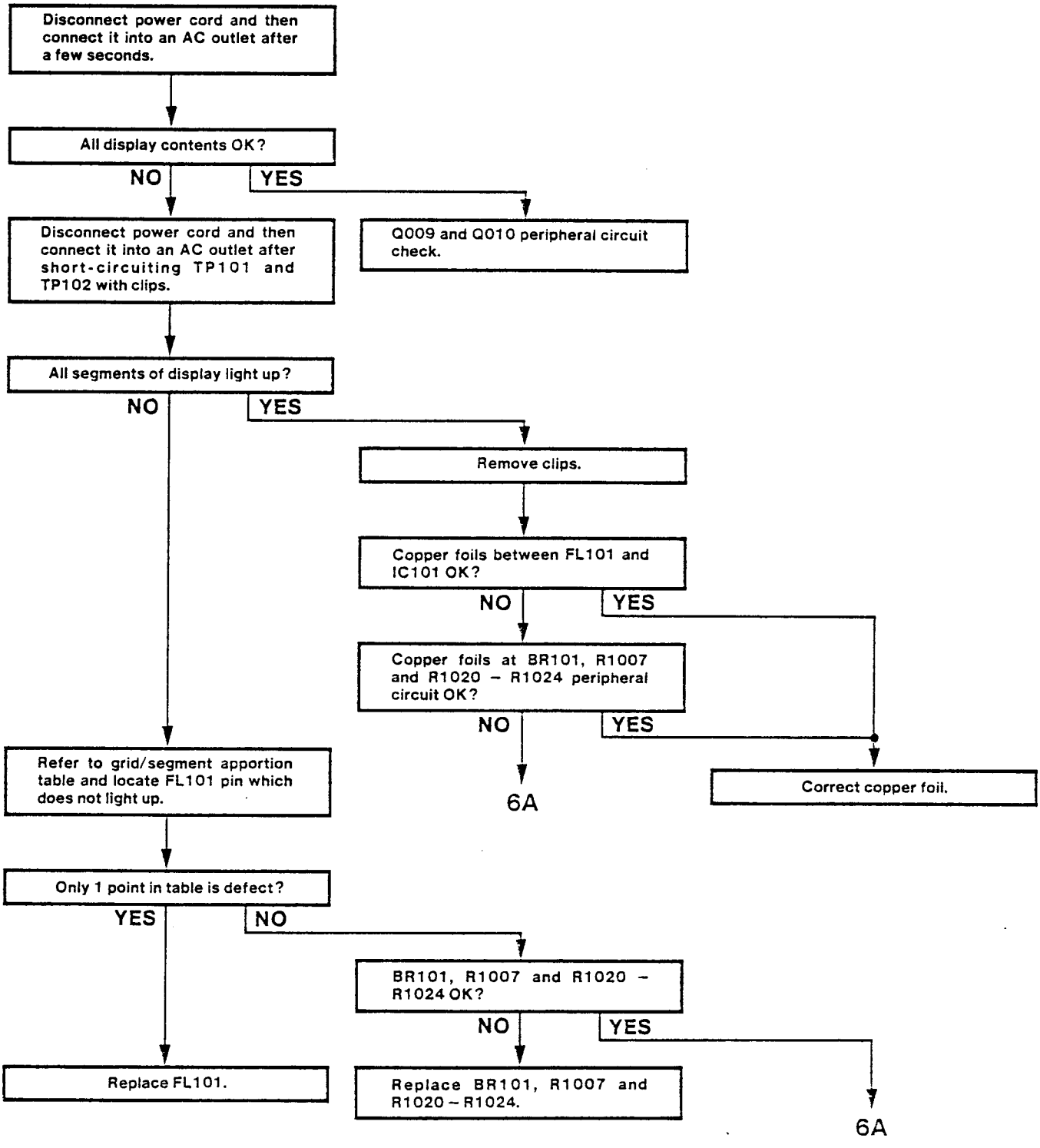
5-6. TIMER CIRCUIT

Step 1. FL display tube is defect.

1. All displays do not light up.

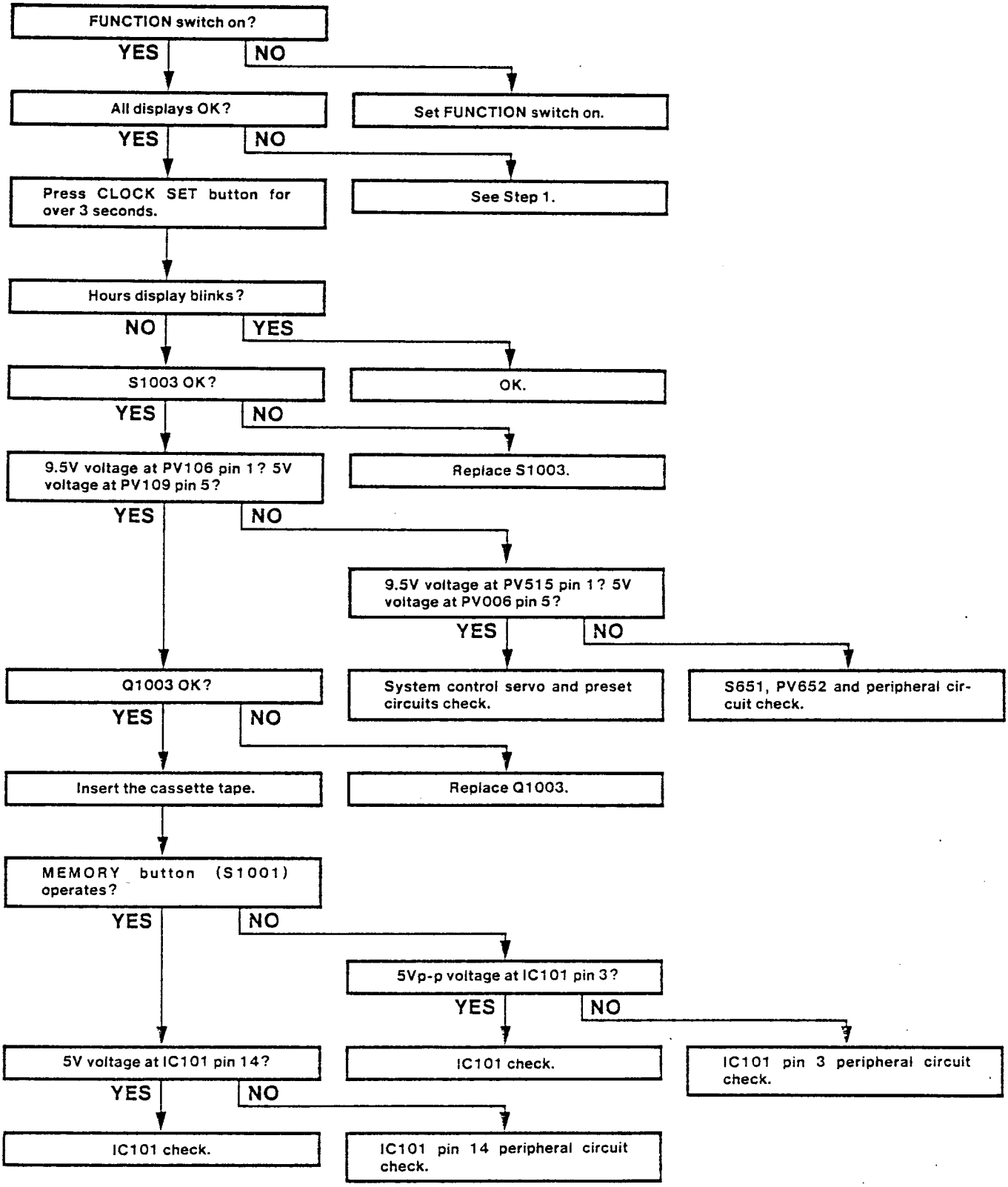


2. Display contents is defect.

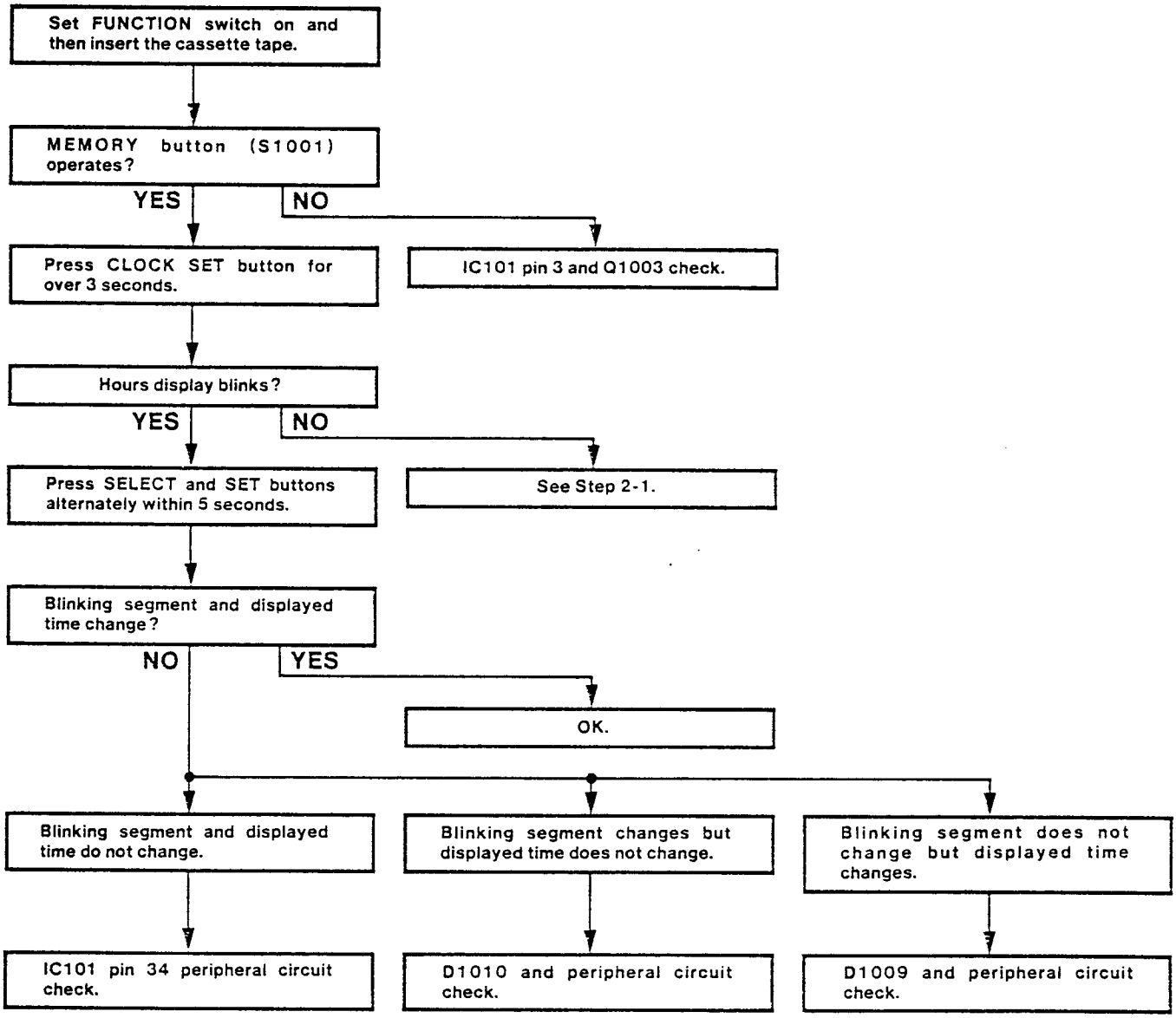


Step 2. Clock setting is not possible.

1. CLOCK SET button (S1003) does not operate.

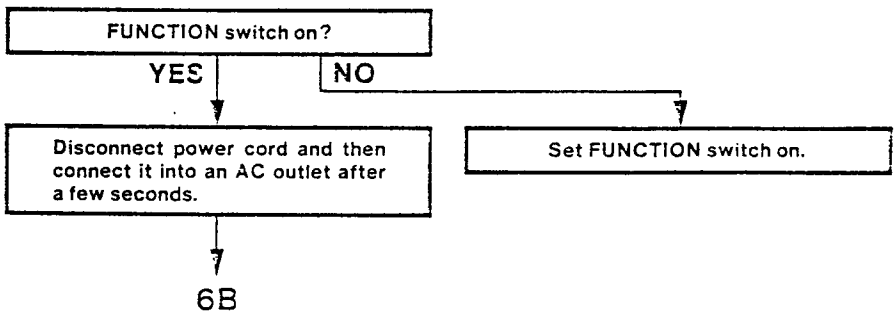


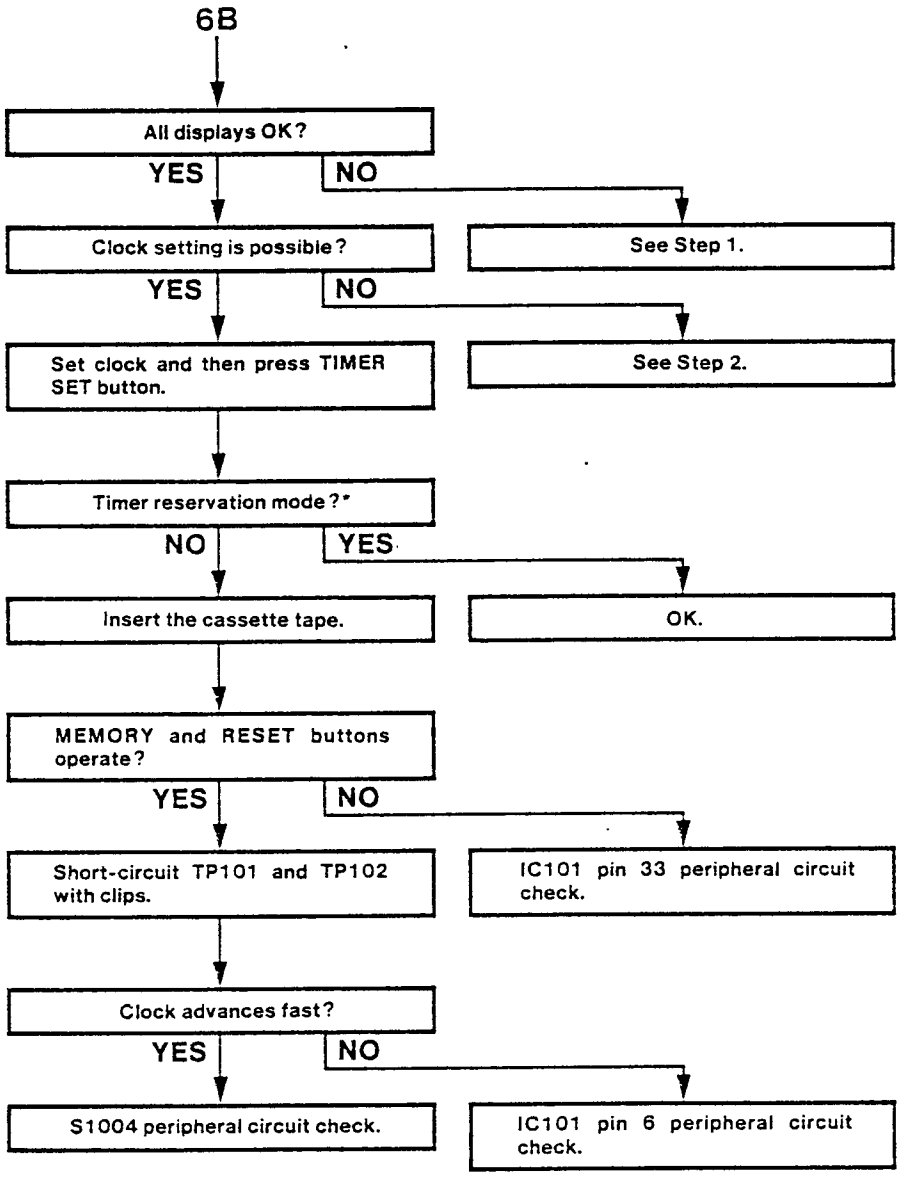
2. SELECT (S1005) or SET (S1006) button does not operate.

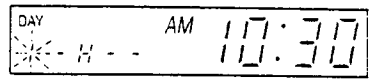


Step 3. Timer reservation is not possible.

1. When TIMER SET button (S1004) is pressed, the unit does not enter the timer reservation mode.

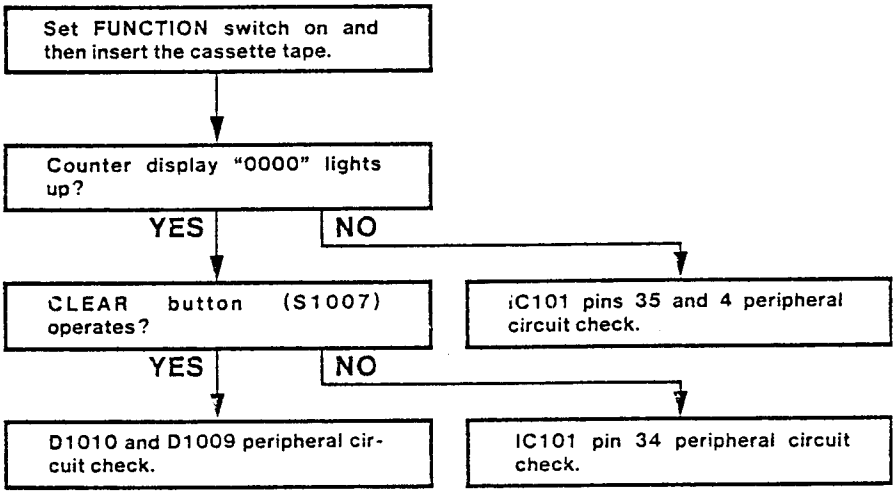






* Timer reservation mode display

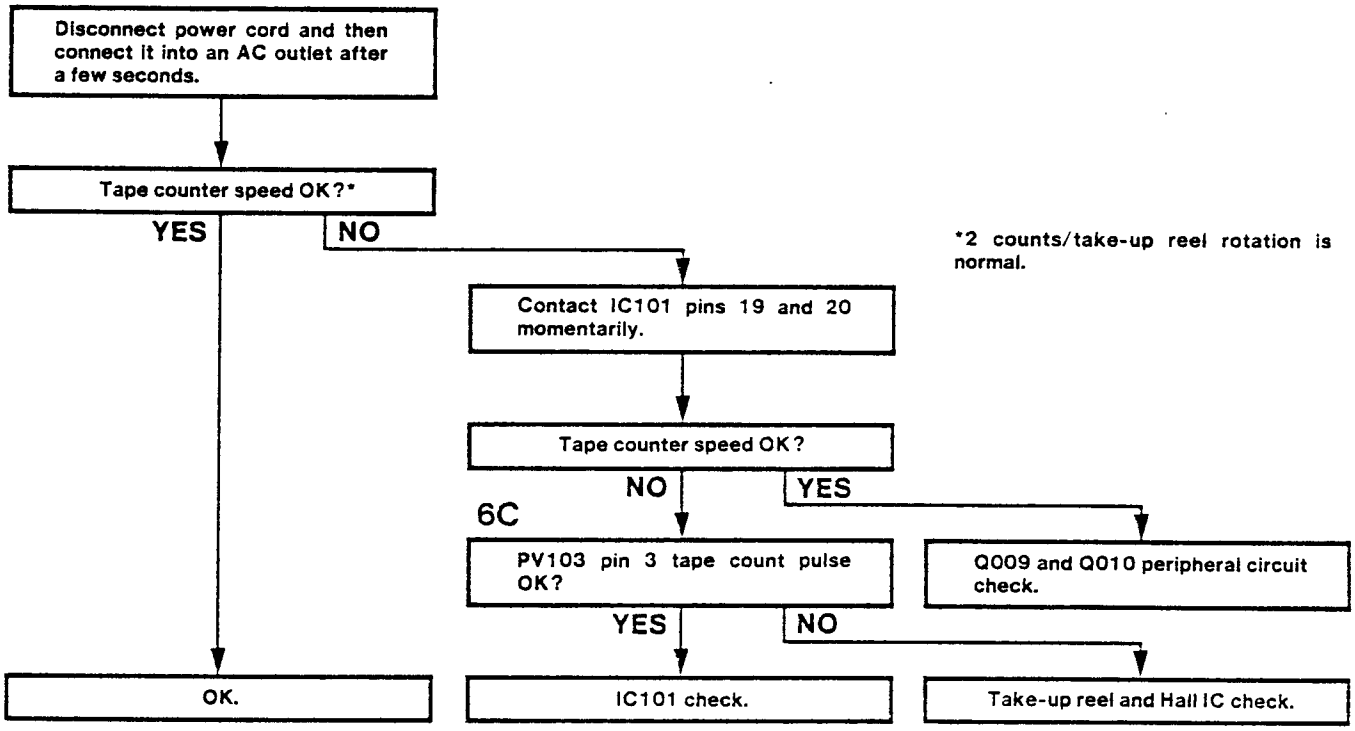
2. SELECT or SET button does not operate.



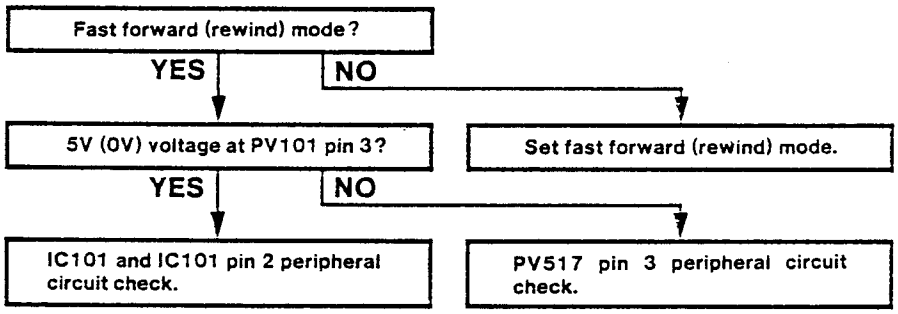
Note: If display indicates "DAY 1", times earlier than the present time cannot be entered. Recording time is automatically cancelled when display indicates "0H00".

Step 4. Tape counter is defect.

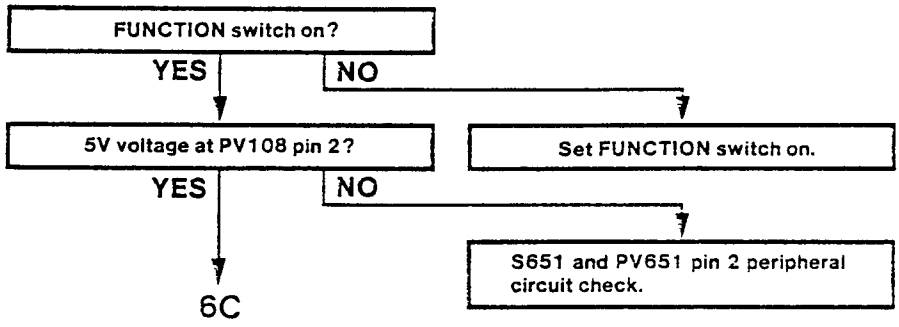
1. Counting speed is too quick or irregular.



2. Tape counter does not count up or down consistently.

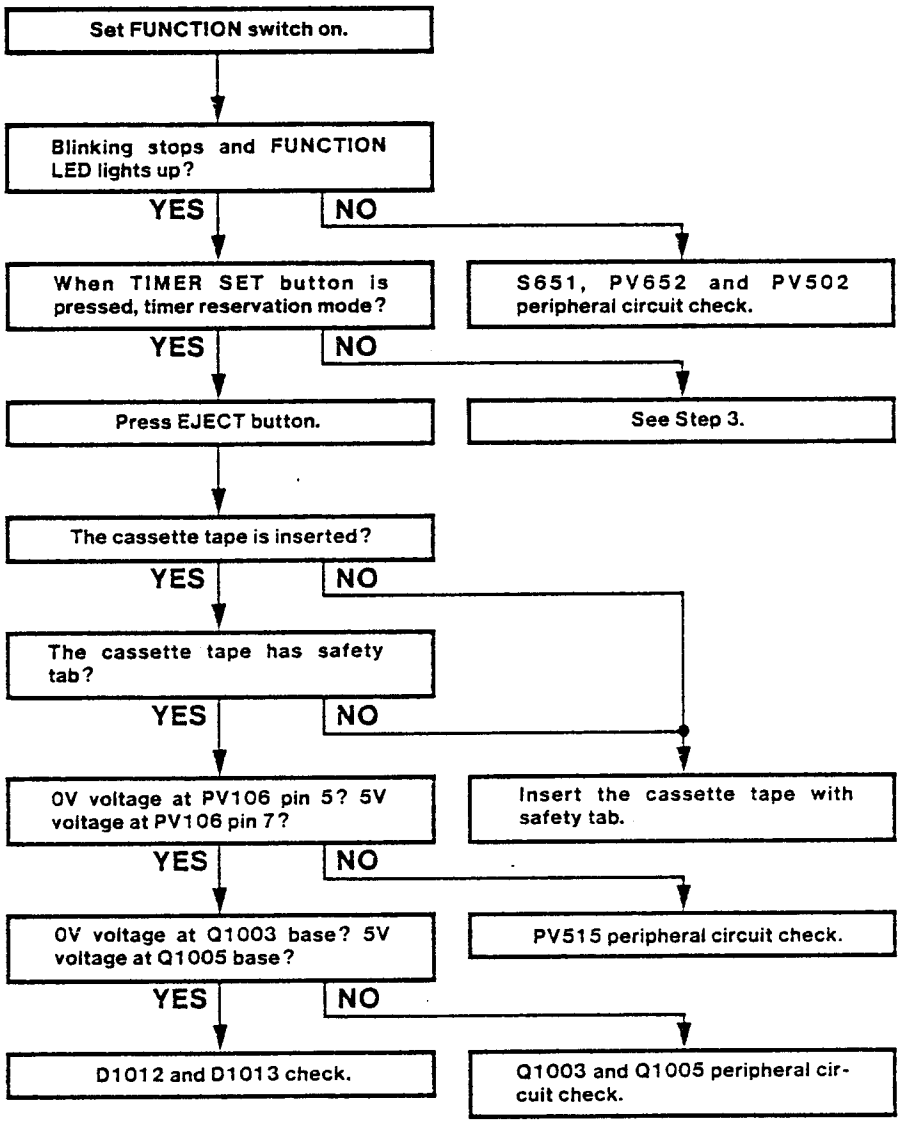


3. Tape counter does not count at all.

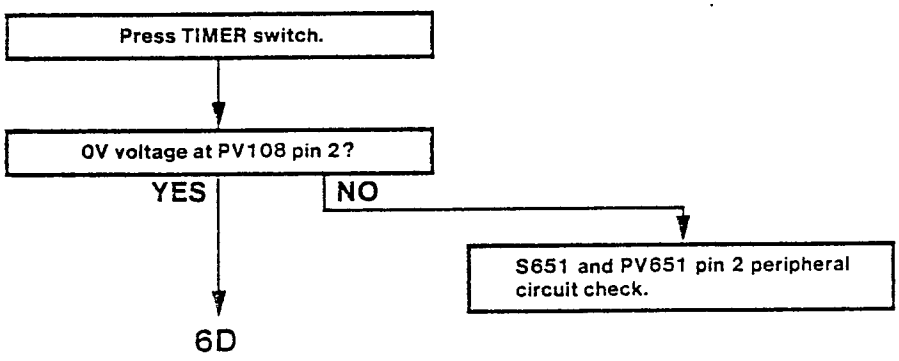


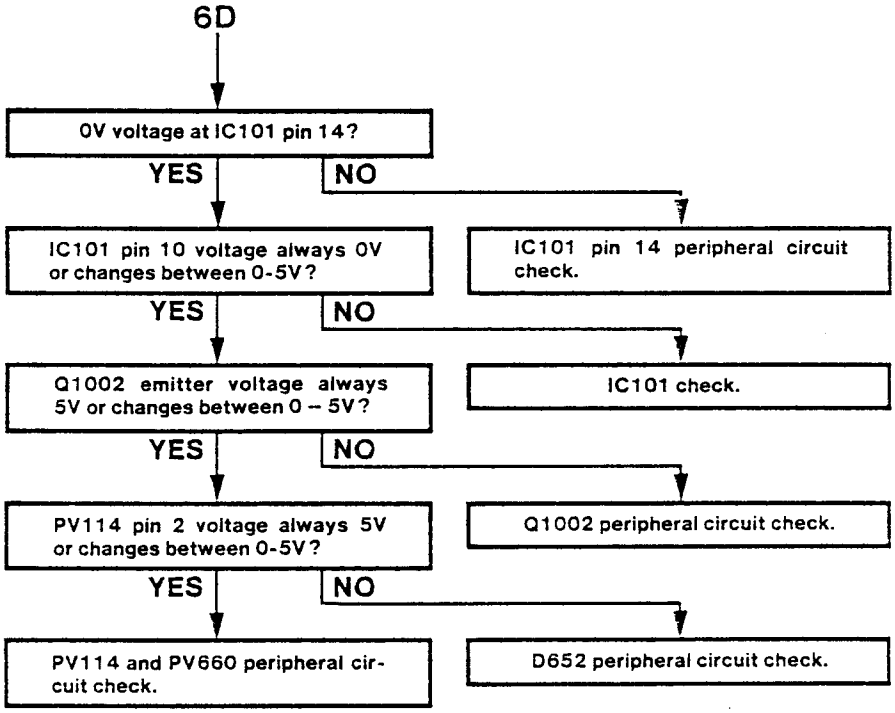
Step 5. TIMER LED does not light up.

1. TIMER LED blinks but does not light up.

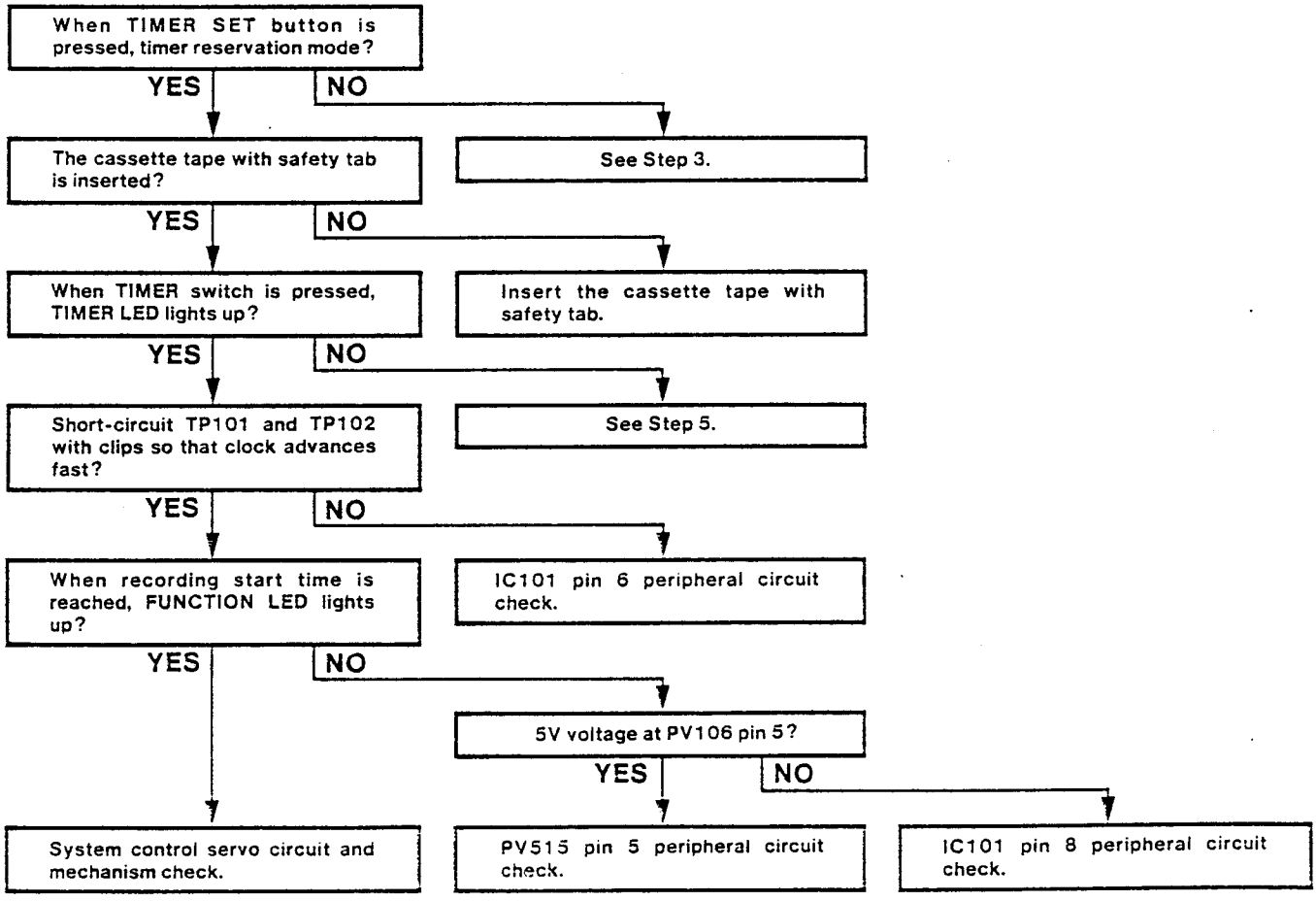


2. TIMER LED does not blink or light up.

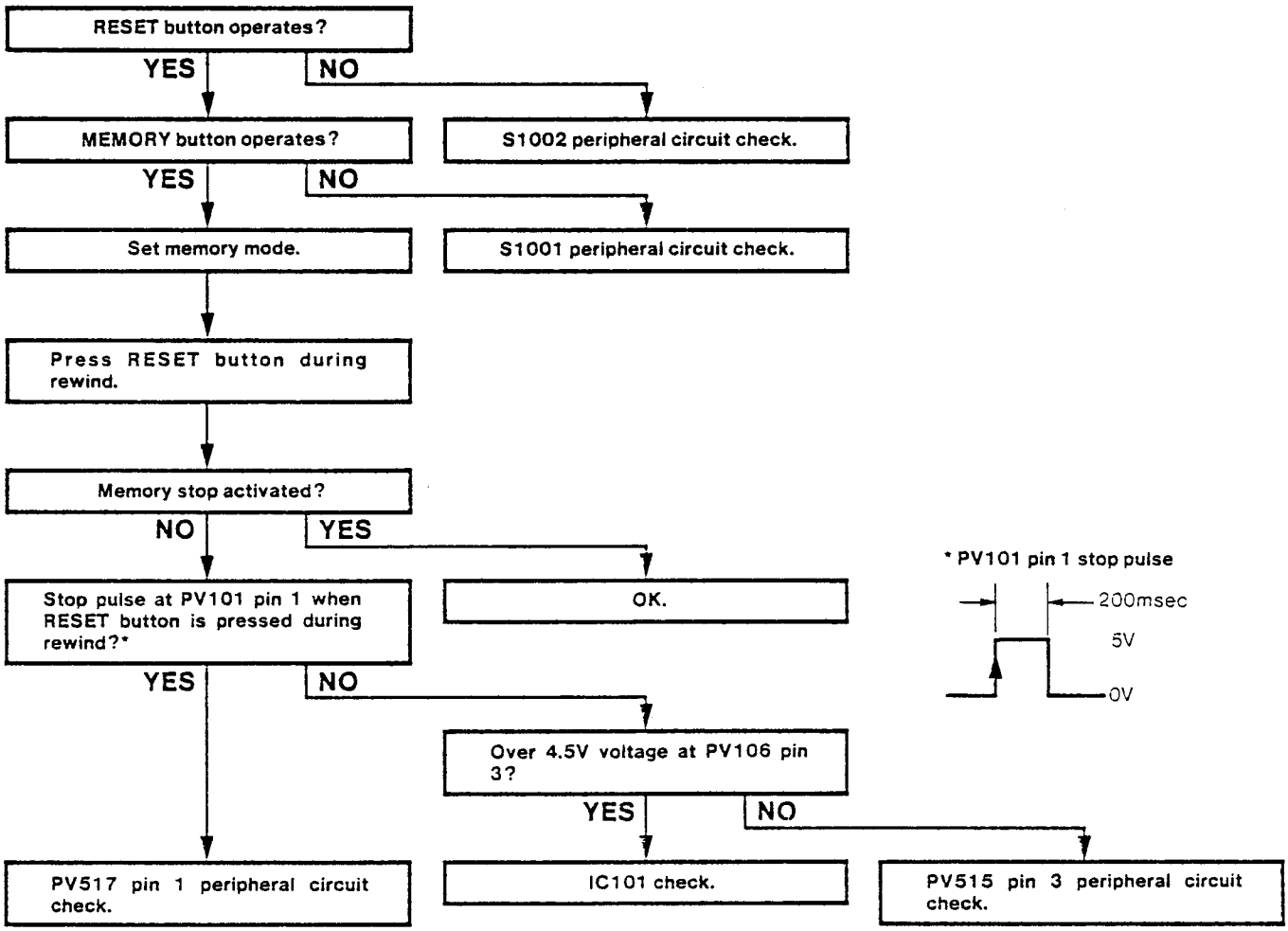




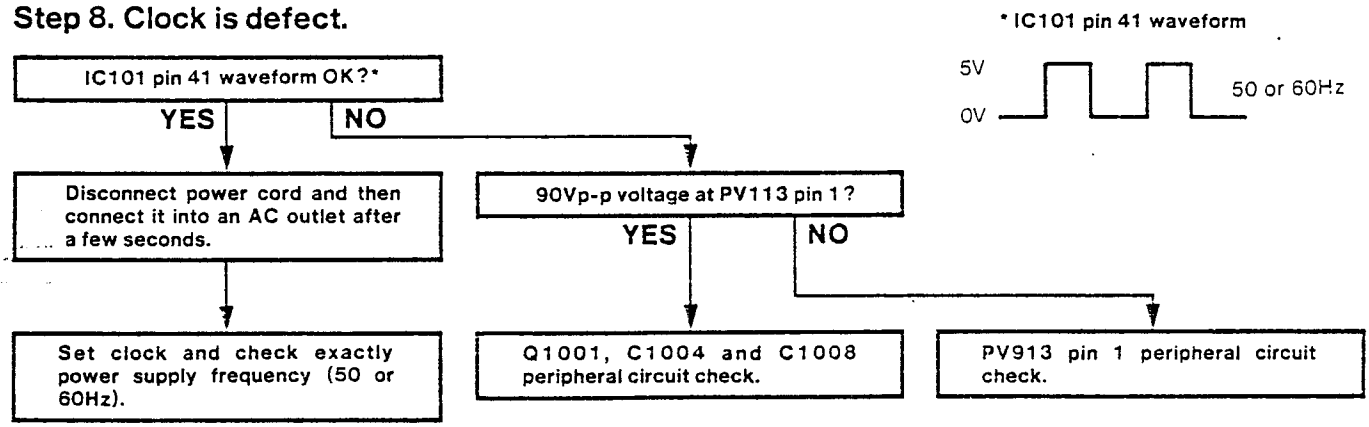
Step 6. Timer recording is not possible.



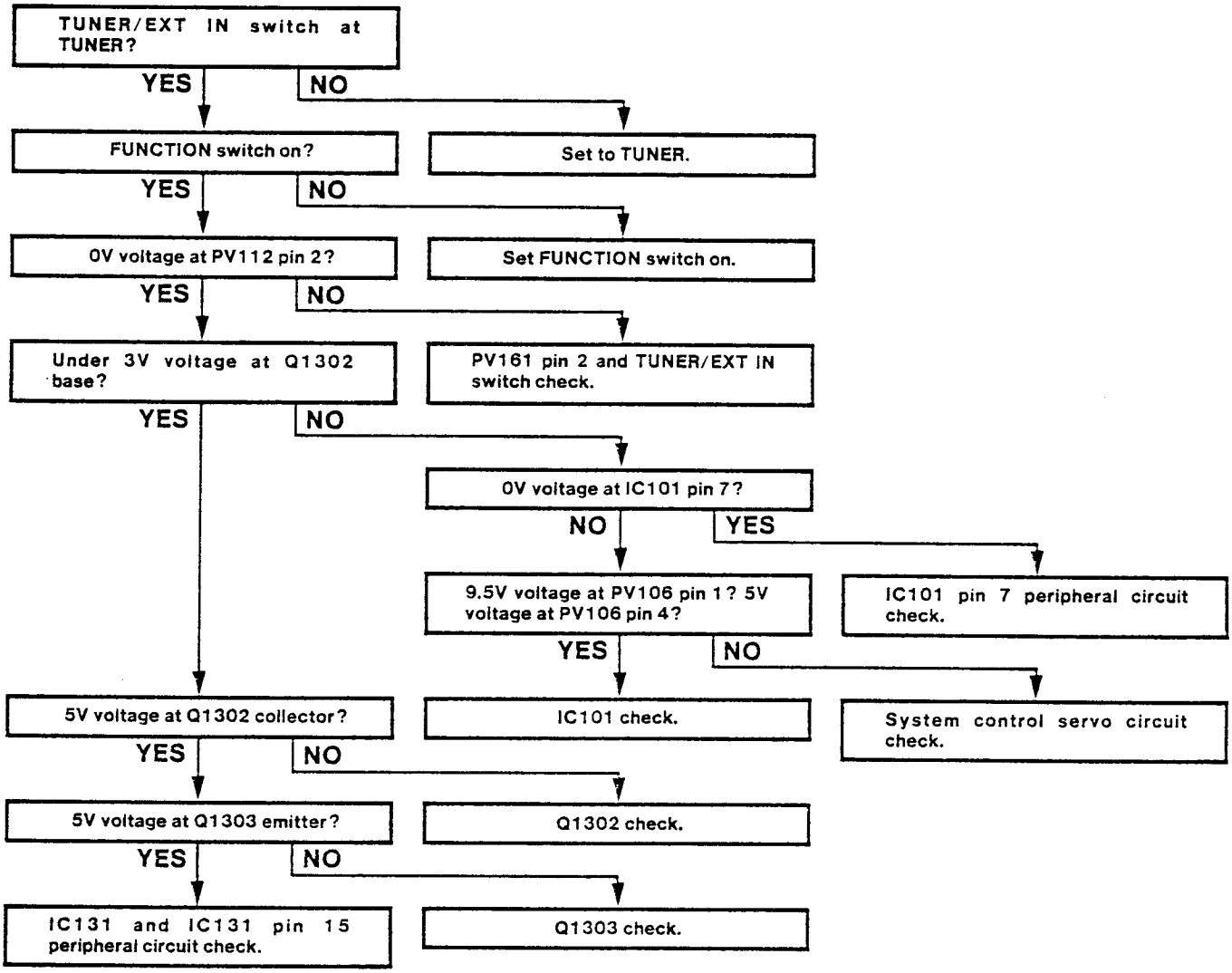
Step 7. Memory stop is not possible.



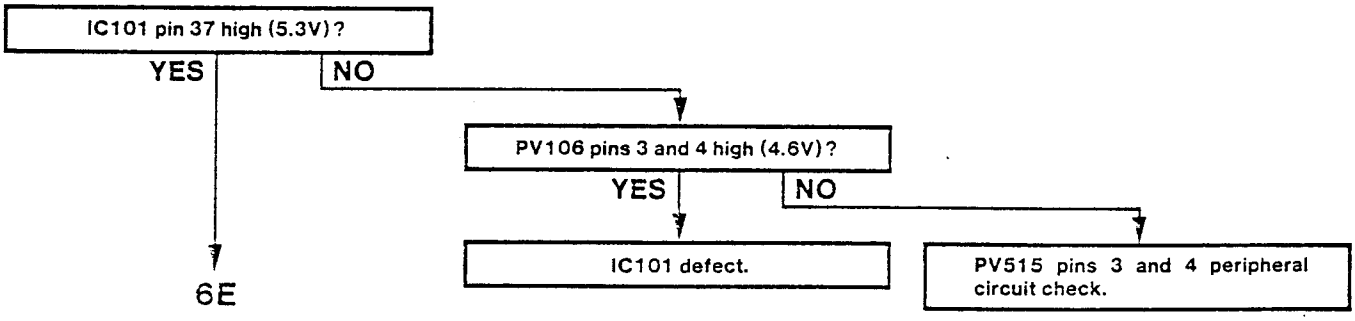
Step 8. Clock is defect.

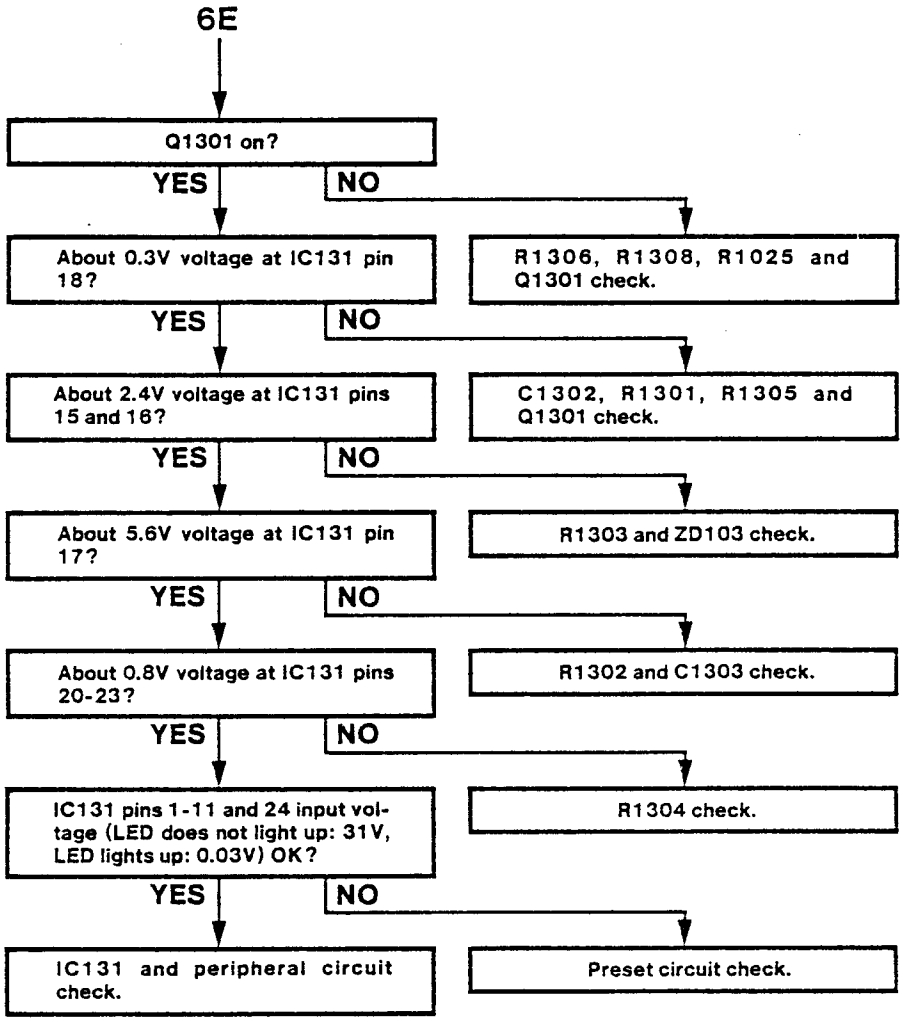


Step 9. CHANNEL LED does not light up.

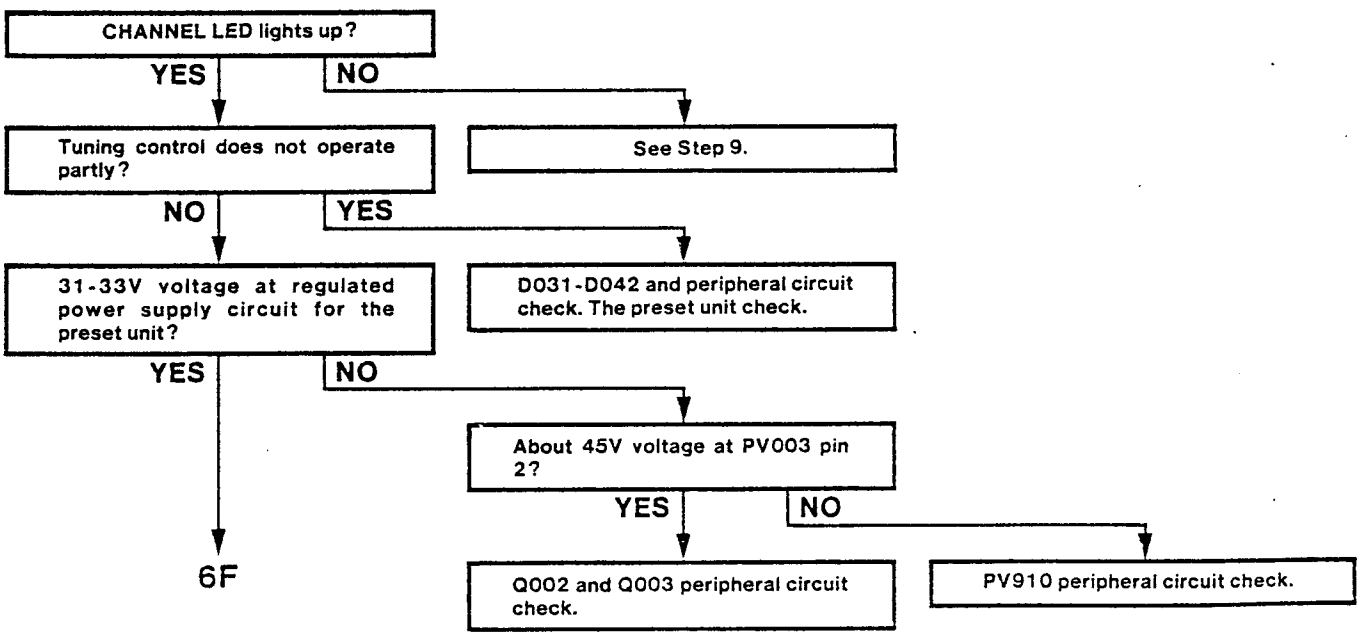


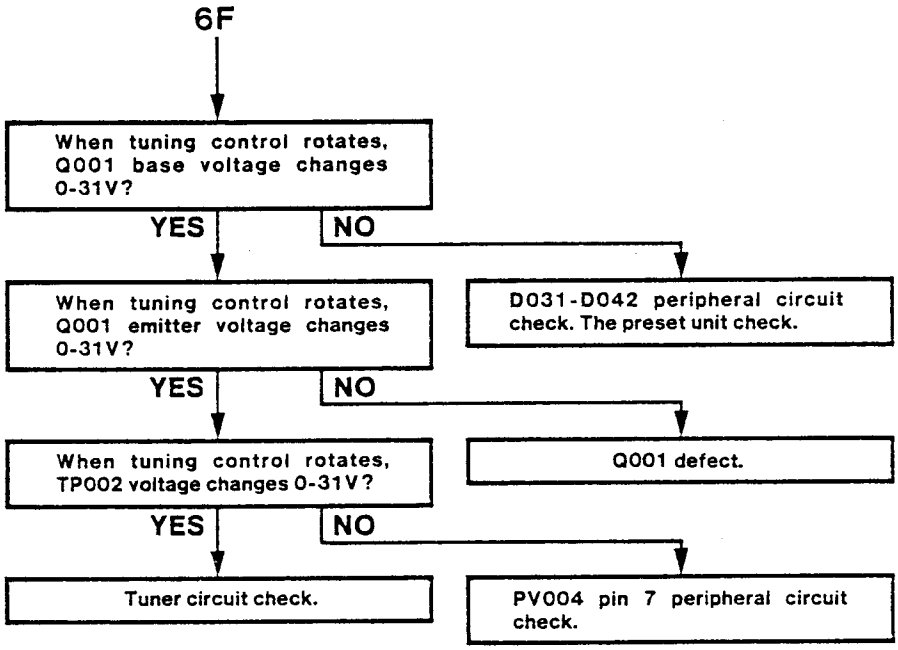
Step 10. Channel selector is defect.



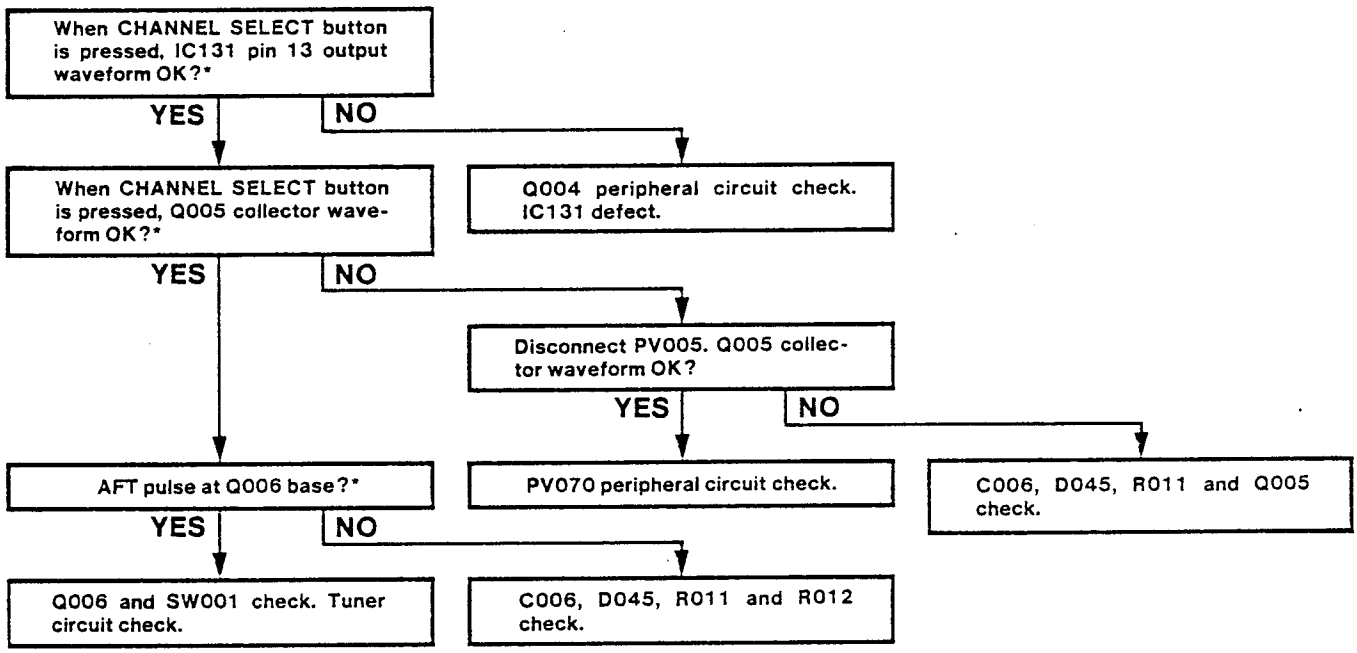


Step 11. Channel tuning is not possible.

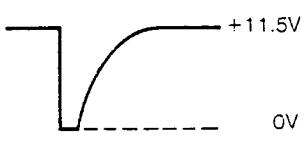




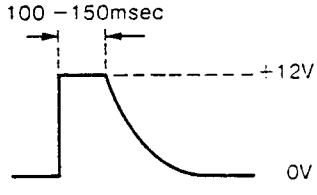
Step 12. AFT is defect.



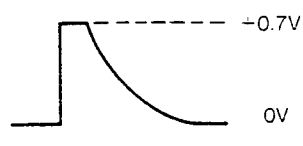
* IC131 pin 13 output waveform



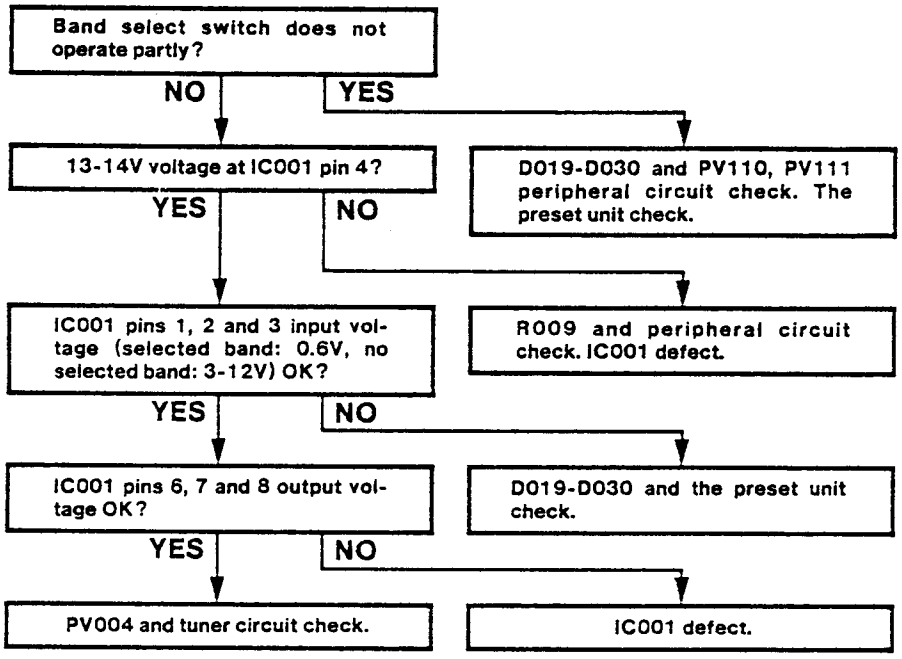
* Q005 collector waveform



* Q006 base AFT pulse

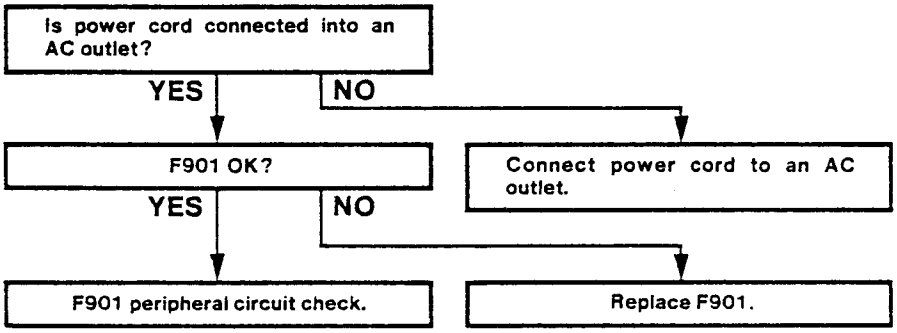


Step 13. Band selector is defect.

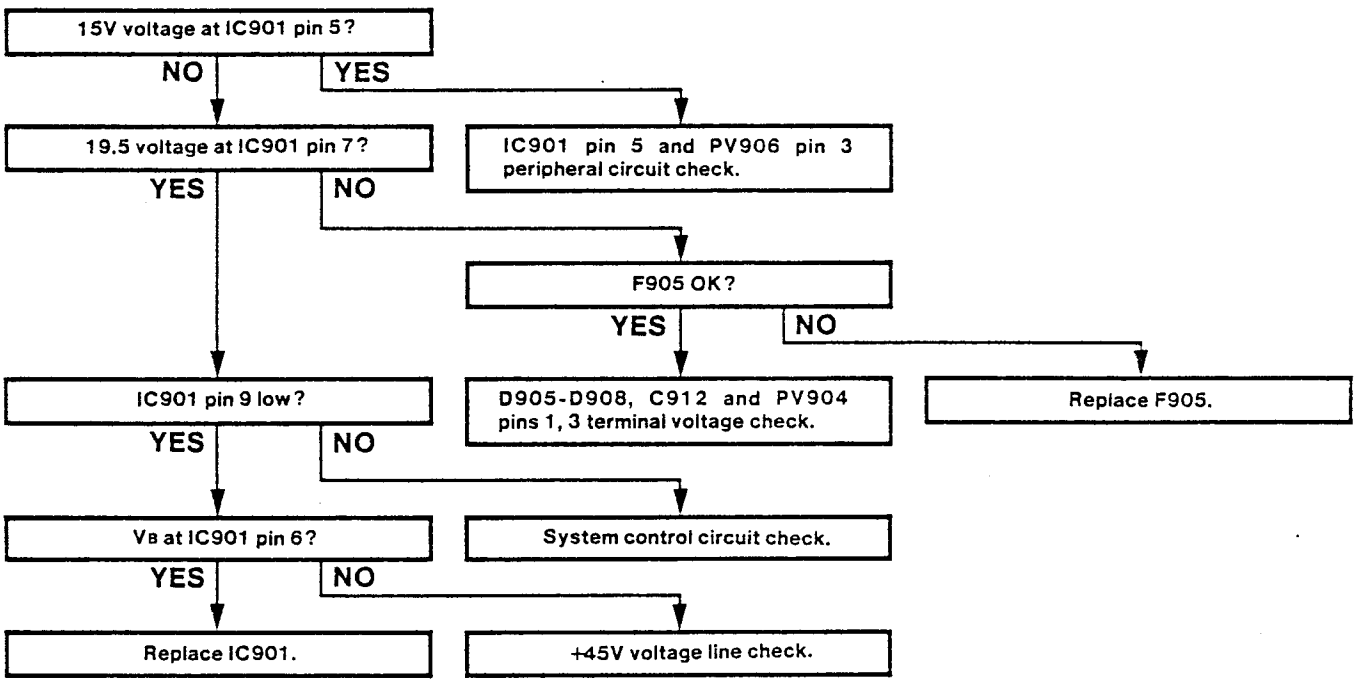


5-7. POWER SUPPLY CIRCUIT

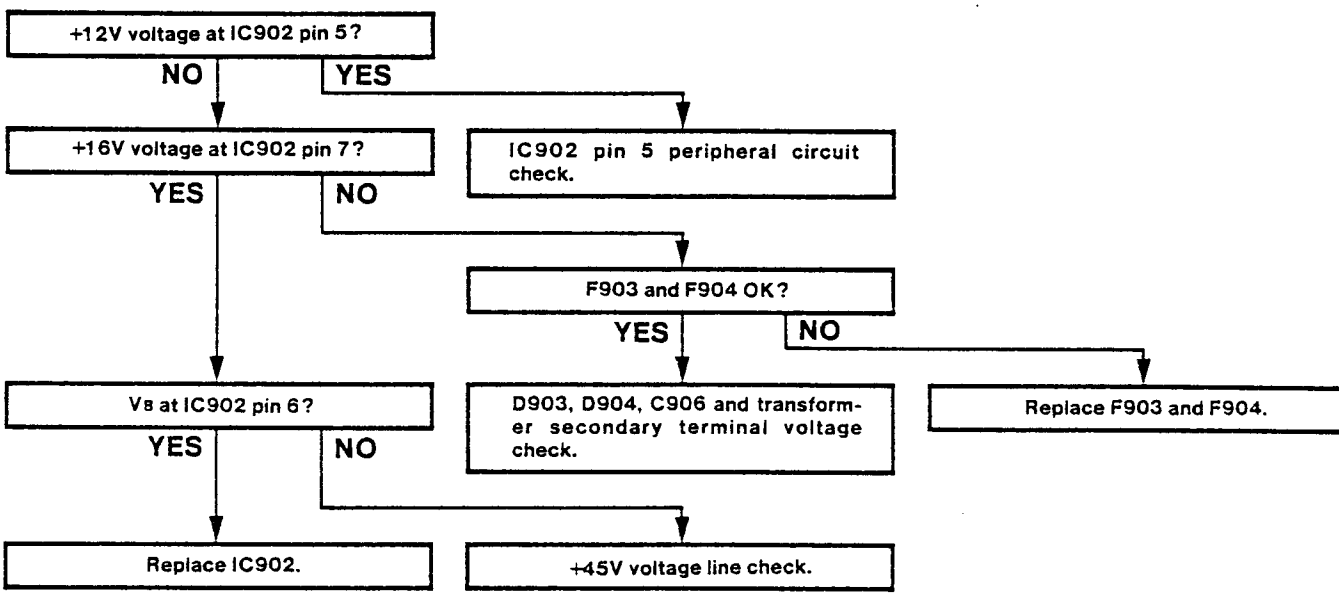
Step 1. No power supply.



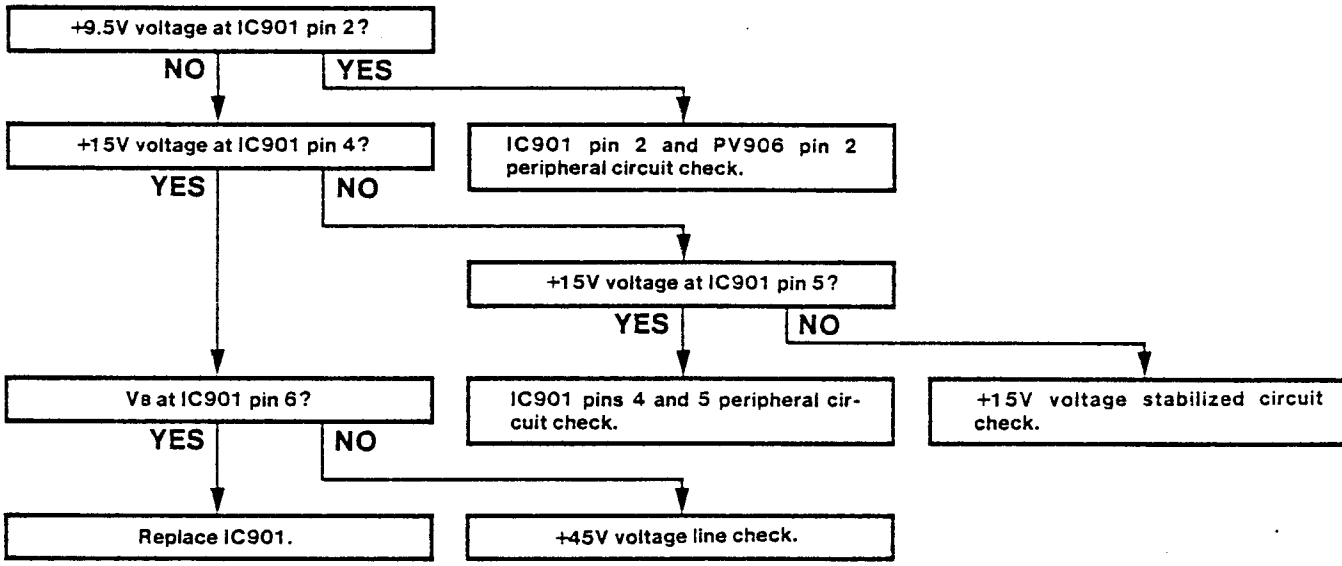
Step 2. No +15V.



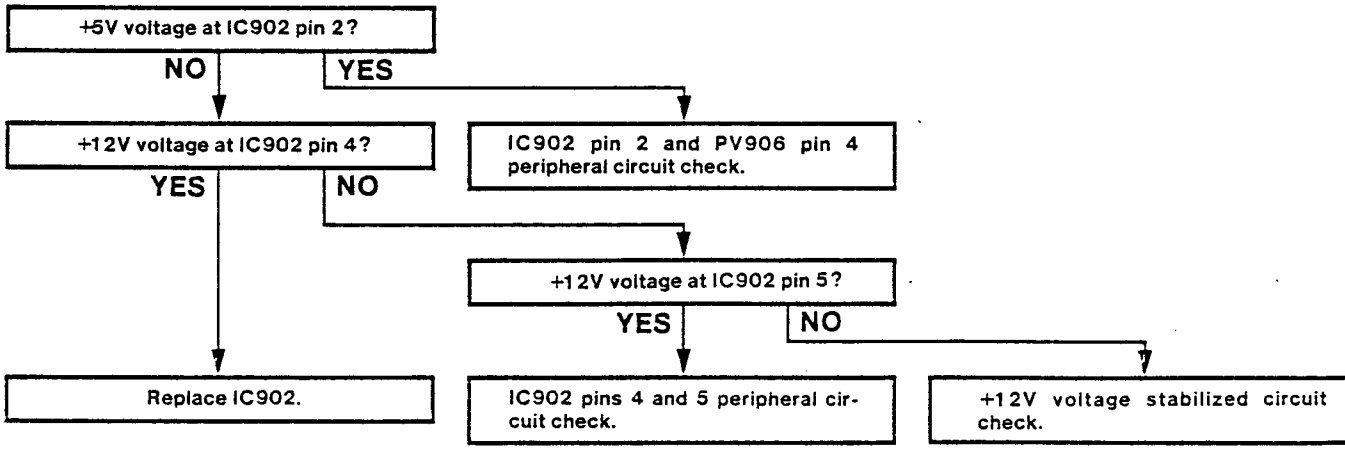
Step 3. No +12V.



Step 4. No +9.5V.



Step 5. No +5V.

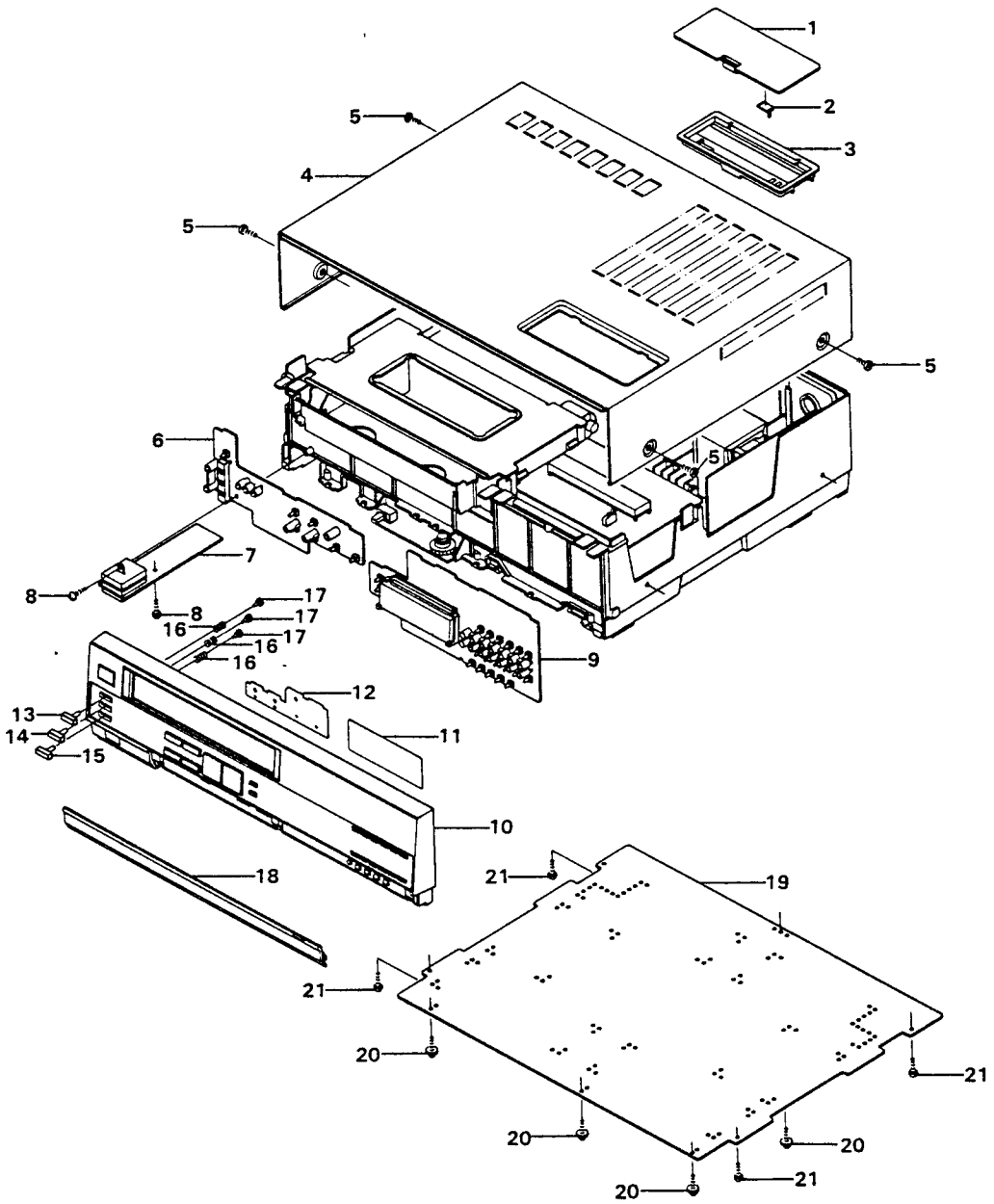


CABINET PARTS (1)

Ref No	Part No.	Description
1	143-0-1454-00610	Door Preset Assy-HAC-G
2	143-2-6104-02300	Slide, AFT Switch-HAB
3	143-2-1204-00906	Case, Preset-HAC-B2
4	143-0-1254-00201	Top Cover Assy-HAC-B
5	101-3-1704-00814	Screw, Bind Hd Machine +M4X8
6	0-4014-01902	Key Function PC Assy
7	0-4014-02400	Wireless PC Assy
8	103-3-1903-01011	Screw, Brazier Hd Tapping +M3X10
9	0-4014-01643	Timer PC Assy
10	143-0-1104-00711	Cabinet Front Assy-HAC-H
11	143-2-1504-01400	Filter FL-HAB

Ref No	Part No.	Description
12	143-2-3704-00300	Light Shelter-HAC-V
13	143-2-1704-08101	Button Power-HAC-A1
14	143-2-1704-08201	Button Power-HAC-B1
15	143-2-1704-08301	Button Power-HAC-C1
16	143-2-6704-02100	Spring, Button-HAB
17	143-2-1704-08400	Flange, Button-HAC
18	143-0-1454-00508	Door Front Assy-HAC-G
19	143-2-1354-00400	Bottom, Cover-HAC
20	143-2-5804-01400	Flange Screw, 3X12
21	116-3-1703-00811	Screw, Bind Hd Tapping B-Tite +M3X8

NOTE: Parts order must contain Model Number, Part Number and Description.

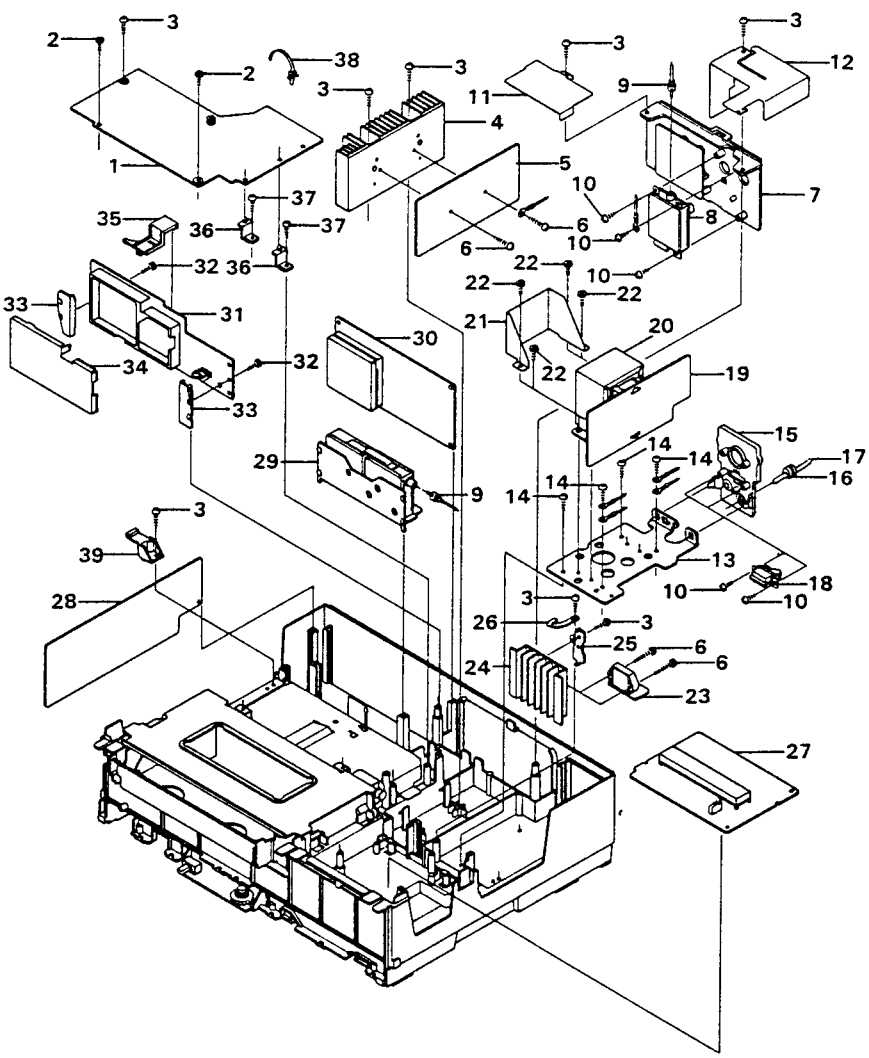


CABINET PARTS (2)

Ref No	Part No.	Description
1	0-4014-02280	Chrominance PC Assy
2	101-3-1703-00611	Screw, Bind Hd Machine +M3X6
3	103-3-1903-01011	Screw, Brazier Hd Tapping +M3X10
4	143-0-7904-00500	Radiator Assy-HAC
5	0-4014-01713	Power B, PC Assy
6	103-3-1903-01611	Screw, Brazier Hd Tapping +M3X16
7	0-4014-01731	Rear Terminal PC Assy
8	4-1164-01250	RF, Converter-M
9	0-4034-00010	Wire Shield Assy
10	103-3-1903-00811	Screw, Brazier Hd Tapping +M3X8
11	143-2-3604-01500	Insulator, Plate-HAC
12	143-2-3604-01100	Insulator, Cover-HAC
13	143-2-3404-09100	Brkt, Power Trans-HAC
14	103-3-1904-01211	Screw, Brazier Hd Tapping +M4X12
15	143-2-1304-00701	Power, Terminal Board-HAC-L
16	143-2-6104-02400	HEYCO, Bush-SR-4K-4
17	0-4054-00100	Power Cord Assy (U.K.)
18	4-2314-00240	See Switch
19	0-4014-01703	Power A, PC Assy
20	4-2514-00603	Power, Transformer
21	143-2-3504-05900	Shield, Plate Trans-HAC

Ref No	Part No.	Description
22	116-3-1704-00811	Screw, Brazier Hd Tapping B-Tite +M4X8
23	0-4014-01720	Power C, PC Assy
24	143-2-7904-01900	Radiator-HAC
25	143-2-3404-10000	Brkt, Rad Mounting-HAC-C
26	143-2-5854-00300	Wire, Clamp
27	0-4014-02251	Preset PC Assy
28	0-4014-02132	Servo Adjust PC Assy
29	4-1154-02250	Tuner, IF Unit
30	0-4014-02240	Audio PC Assy
31	0-4014-02270	Head Amp PC Assy
32	116-3-1703-00611	Screw, Brazier Hd Tapping B-Tite +M3X6
33	143-2-3404-09900	Brkt, PB Mounting-HAC
34	143-2-3504-06100	Shield Head Amp Top-HAC
35	143-2-3404-09800	Holder, P.C.B.-HAC-D
36	143-2-7404-00500	P.C.B. Hinge-C
37	103-3-1903-01211	Screw, Brazier Hd Tapping +M3X12
38	143-2-5854-01600	Snap, Band-KSG130
39	143-2-3404-08701	Holder, P.C.B.-HAC-A

NOTE: Parts order must contain Model Number, Part Number and Description.

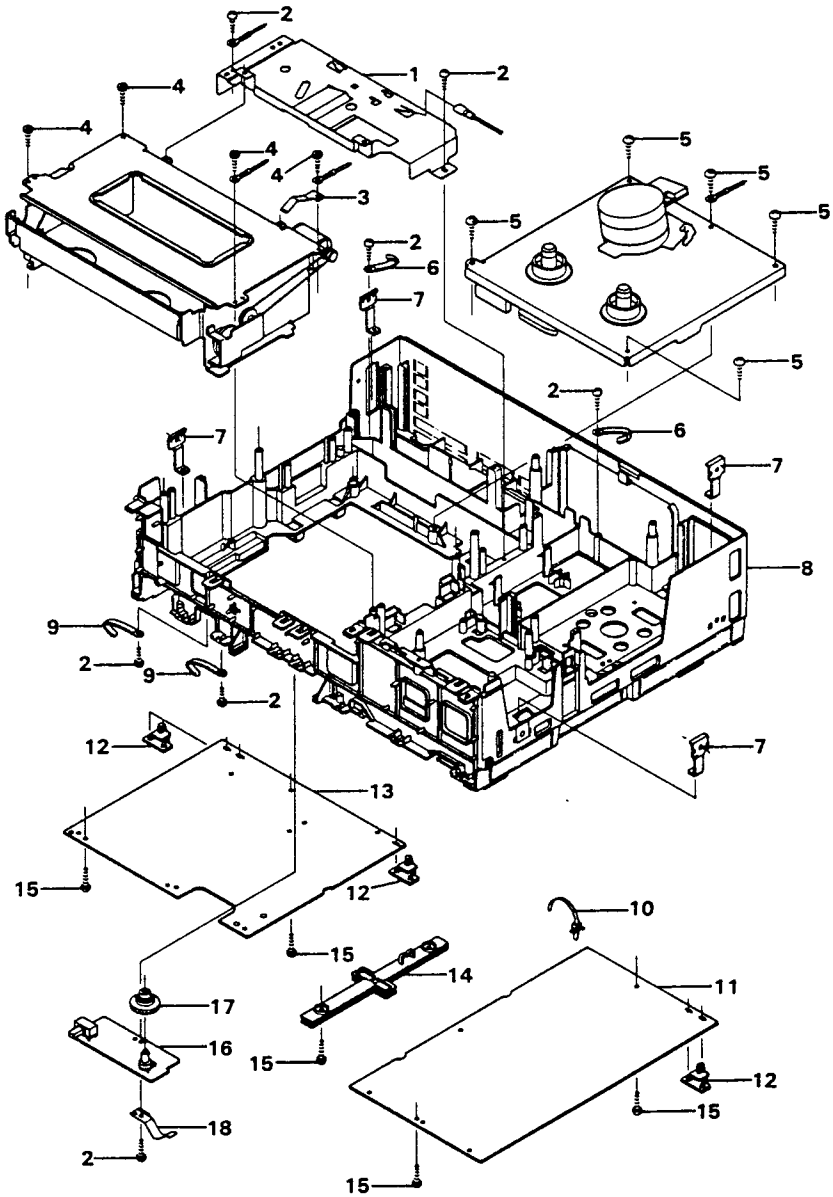


CABINET PARTS (3)

Ref No	Part No.	Description
1	143-2-3504-05600	Shield, Plate-HAC-B
2	103-3-1903-01011	Screw, Brazier Hd Tapping +M3X10
3	143-2-6904-02000	Ground, Plate Top-HAC
4	103-3-1703-01211	Screw, Brazier Hd Tapping +M3X12
5	103-3-1804-01211	Screw, Tras Hd Tapping +M4X12
6	143-2-5854-00300	Wire, Clamp
7	143-2-3404-09000	Brkt, Top Cover-HAC
8	143-0-1304-00411	Cabinet Bottom Assy-HAC-J
9	143-2-5854-00400	Wire, Clamp

Ref No	Part No.	Description
10	143-2-5854-01600	Snap, Band KSG130
11	0-4014-02291	Luminance PC Assy
12	143-2-7404-00200	P.C.B. Hinge-A
13	0-4014-02122	Syscon Servo PC Assy
14	143-2-3304-02101	Base, PB Mounting-HAC
15	103-3-1903-01219	Screw, Brazier Hd Tapping +M3X12
16	0-4014-02181	Tracking VR PC Assy
17	143-2-1704-08500	Knob, Tracking-HAC
18	143-2-6904-02100	Ground, Spring-HAC

NOTE: Parts order must contain Model Number, Part Number and Description.

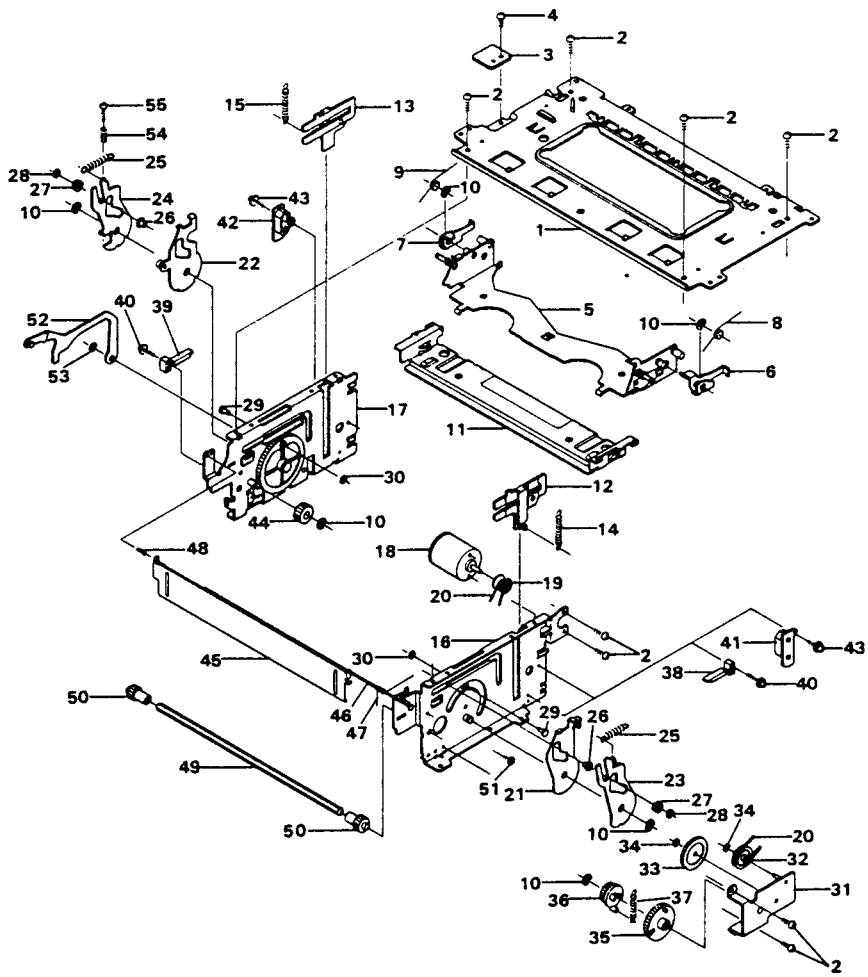


CHASSIS PARTS (1)

Ref No	Part No.	Description
1	143-2-7304-10900	Board, Top
2	101-3-1303-00611	Screw, Pan Hd Machine +M3X6
3	0-4014-01631	Terminate PC Assy
4	101-3-1303-00411	Screw, Pan Hd Machine +M3X4
5	143-0-7304-05500	Tray Assy
6	143-2-7304-11400	Clamper-Right
7	143-2-7304-11300	Clamper-Left
8	143-2-6804-01800	Spring, Clamper-Right
9	143-2-6804-01900	Spring, Clamper-Left
10	112-3-1304-00040	E-Ring, M4.0
11	143-2-7304-11500	Board, Under
12	143-2-7304-12900	Elevator-Right
13	143-2-7304-12800	Elevator-Left
14	143-2-6604-05000	Spring, Elevator-Right
15	143-2-6604-04700	Spring, Elevator-Left
16	143-0-7304-05700	Board Side Right Assy
17	143-0-7304-05600	Board Side Left Assy
18	4-5254-00230	Front, Loading Motor
or	4-5254-00231	Front, Loading Motor
19	143-2-7304-13800	Pulley, Motor
20	143-2-7504-00500	Belt
21	143-2-7304-12100	Plate, Swing-Right
22	143-0-7304-05800	Plate Swing Left Assy
23	143-2-7304-12300	Lever, Swing-Right
24	143-2-7304-12200	Lever, Swing-Left
25	143-2-6604-04800	Spring, Swing
26	143-2-7304-13300	Roller, Tray (A)
27	143-2-7304-13400	Roller, Tray (B)
28	112-3-1302-30040	E-Ring, M2.3
29	143-2-7304-14300	Roller, Swing

Ref No	Part No.	Description
30	112-3-1302-00040	E-Ring, M2.0
31	143-0-7304-05300	Base Gear Assy
32	143-2-7304-13600	Pulley, Pinion
33	143-2-7304-12700	Gear, Reduction
34	112-3-1301-50040	E-Ring, M1.5
35	143-2-7304-13000	Gear, Joint
36	143-2-7304-12600	Gear, Idler
37	143-2-6604-04900	Spring, Eject
38	0-4064-00420	Stop Switch Assy
39	0-4064-00410	Start Switch Assy
40	136-3-1302-01011	Screw, Pan Hd Machine Combination Spring Washer & Plain Washer +M2X10
41	0-4014-01780	EST Assy
42	0-4014-01790	ESS Assy
43	137-3-1302-60411	Screw, Pan Hd Machine Combination Flat Washer M2.6X4
44	143-2-7304-13700	Gear, Idler-Left
45	143-2-7304-11712	Flap-HAC-A12
46	143-2-7304-14200	Shaft, Door
47	143-2-6804-01700	Spring, Door
48	143-2-6704-03300	Spring, Door
49	143-2-7304-14000	Lod, Connect
50	143-2-7304-12500	Gear, Pinion
51	101-3-1703-00311	Screw, Bind Hd Machine +M3X3
52	143-0-7304-05400	Opener Assy
53	112-3-1302-50040	E-Ring, M2.5
54	143-2-6704-03400	Spring, Adjust
55	143-2-5804-03100	Screw, Adjust

NOTE: Parts order must contain Model Number, Part Number and Description.

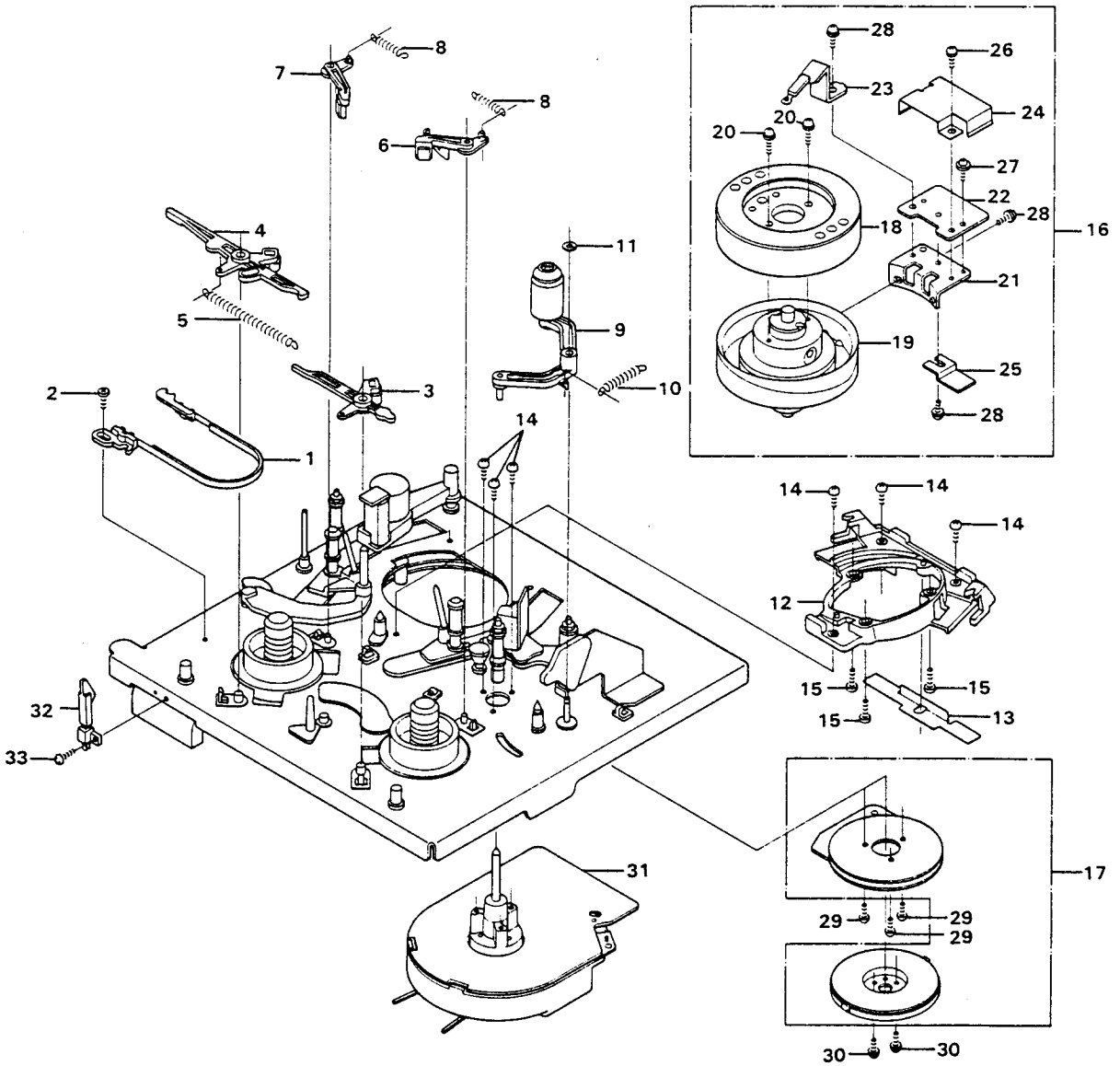


CHASSIS PARTS (2)

Ref No	Part No.	Description
1	143-2-5204-01500	Band, Brake
2	101-3-1702-60411	Screw, Bind Hd Machine +M2.6X4
3	143-0-5204-00700	Main Brake Take Up Assy
4	143-0-5204-00600	Main Brake Supply Assy
5	143-2-6604-02800	Spring, Main Brake
6	143-0-5204-00500	Sub Brake Take Up Assy
or	143-0-5204-01200	Sub Brake Take Up Assy
7	143-0-5204-00400	Sub Brake Supply Assy
or	143-0-5204-01100	Sub Brake Supply Assy
8	143-2-6604-04300	Spring, Sub Brake
9	143-0-4604-00700	Pinch Roller Final Assy
10	143-2-6604-04400	Spring, Pinch Tension
11	143-2-6304-01800	Washer, Stopper 2.5X6X0.25
12	143-0-3404-00800	Base Cylinder Assy
or	143-0-3404-02200	Base Cylinder Assy
13	143-2-5604-04800	Spacer, BC
14	101-3-1302-60611	Screw, Pan Hd Machine +M2.6X6
15	101-3-1703-00611	Screw, Bind Hd Machine +M3X6
16	143-0-4704-03700	Cylinder, Complete
17	4-5254-00120	Cylinder, Motor

Ref No	Part No.	Description
or	4-5254-00121	Cylinder, Motor
18	143-0-4704-01000	Cylinder Upper Assy
19	143-0-9934-00500	Cylinder Service Assy
20	143-2-5804-00700	Screw, M3X8
21	143-2-4704-03000	Bracket, P.C.B. Cylinder
22	0-4014-02260	Cylinder PC Assy
23	143-0-4704-02000	Earth Plate Assy
24	143-2-3504-05500	Shield, Case
25	4-2454-00050	Dew, Heater
26	135-3-1303-00411	Screw, Pan Hd Machine Combination +M3X4
27	131-3-1302-00511	Screw, Pan Hd Machine Combination +M2X5
28	143-2-5804-00300	Screw, M3X6
29	143-2-5804-02000	Screw, M2.3X5
30	143-2-5804-03000	Screw, Pan Hd Machine Combination Plain Washer +M2.3X5
31	4-5254-00130	Capstan, Motor
32	0-4064-00292	Safety Switch Assy
33	101-3-1302-60511	Screw, Pan Hd Machine +M2.6X5

NOTE: Parts order must contain Model Number, Part Number and Description.

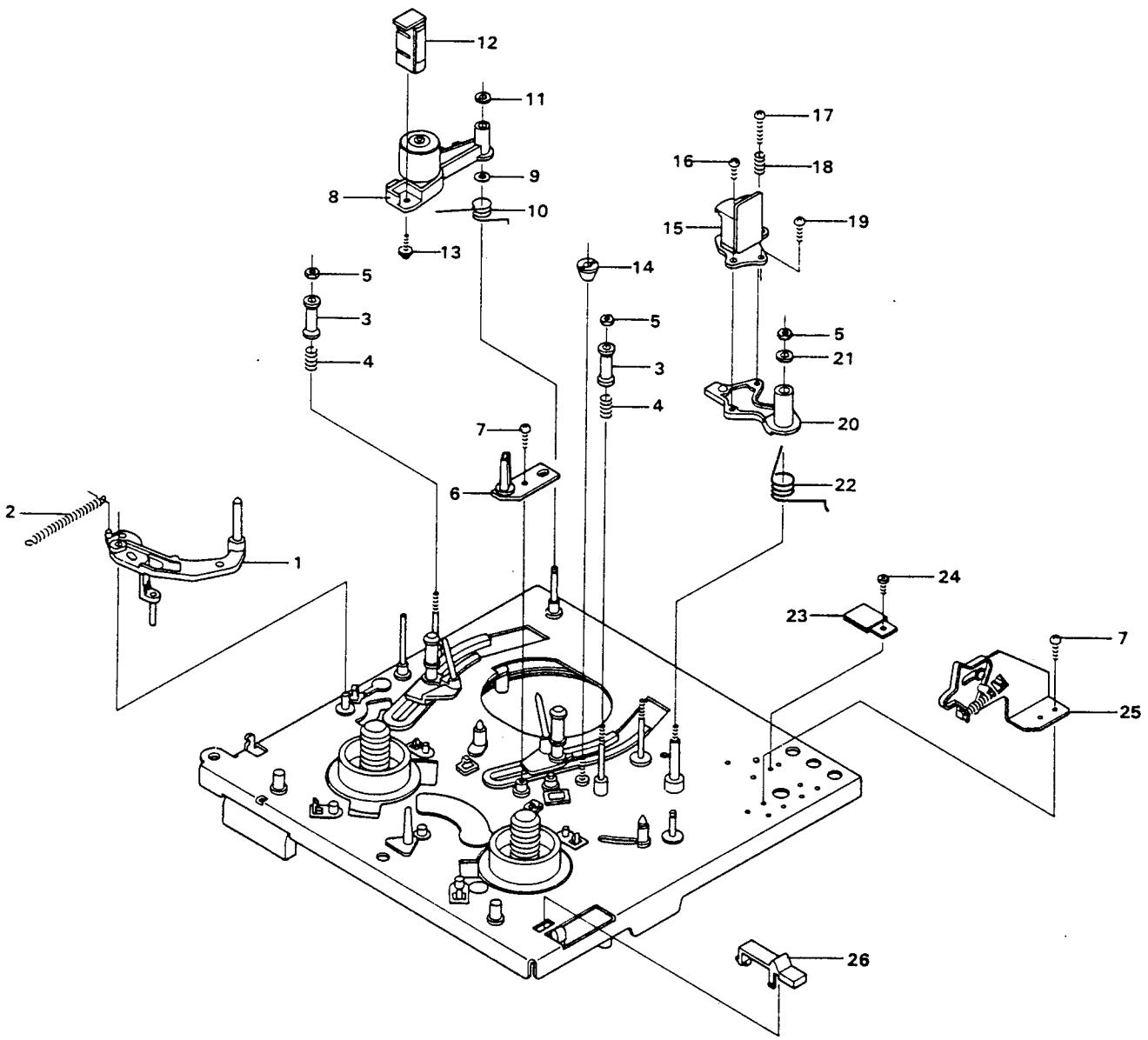


CHASSIS PARTS (3)

Ref No	Part No.	Description
1	143-0-5104-02700	Arm Tension Assy
or	143-0-5104-02800	Arm Tension Assy
2	143-2-6604-04200	Spring, Arm Tension
3	143-2-7704-01800	Guide, Tape
4	143-2-6704-00500	Spring, Adjust Guide
5	106-3-1103-00011	Nut, M3
6	0-4014-01152	End LED PC Assy
7	119-3-1302-60611	Screw, Pan Hd Tapping Del-Tite +M2.6×6
8	143-0-5104-01200	Arm, Impedance Roller Complete
9	143-2-6304-00700	Washer, 3.2×6×0.25
10	143-2-6804-01600	Spring, Arm Impedance
11	143-2-6304-01800	Washer, Stopper 2.5×6×0.25
12	0-4064-00500	Full Erase Hd Assy
13	136-3-1302-00511	Screw, Pan Hd Machine Combination Spring Washer & Plain Washer

Ref No	Part No.	Description
		+M2×5
14	143-2-5704-00400	Nut, Tangential
15	0-4064-00490	Audio Control Erase Hd Assy
16	143-2-5804-02306	Screw, Convex
17	101-3-1302-61211	Screw, Pan Hd Machine +M2.6×12
18	143-2-6704-01600	Spring, Azimuth
19	143-2-5804-02300	Set, Screw
20	143-2-5104-05400	Base, Audio Control Erase Hd
or	143-2-5104-07100	Base, Audio Control Erase Hd
21	143-2-6204-00500	Washer, 3.2×8×1
22	143-2-6704-03200	Spring, Tangential Adjust
23	143-0-3404-01701	Dew Sensor Assy
24	116-3-1702-60611	Screw, Brazier Hd Tapping B-Tite +M2.6×6
25	143-0-7304-05100	Opener, Complete
26	143-2-5104-06500	Lever, Cassette Switch

NOTE: Parts order must contain Model Number, Part Number and Description.

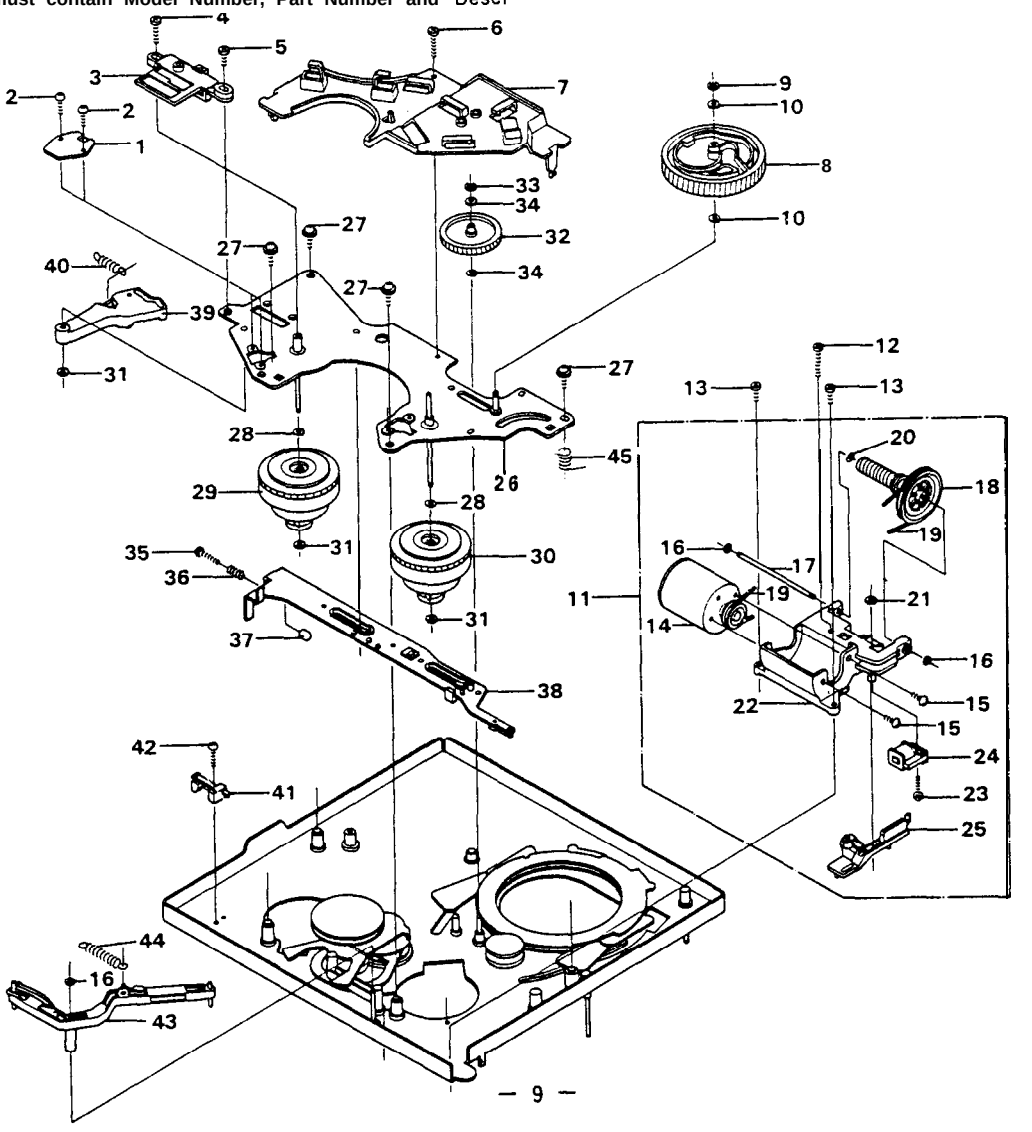


CHASSIS PARTS (4)

Ref No	Part No.	Description
1	O-401 4-01 162	Counter Assy
2	101-3-I 302-00311	Screw, Pan Hd Machine +M2X3
3	4-2314-00250	Mode, Select Switch
4	101-3-I 702-6081 1	Screw, Bind Hd Machine +M2.6X8
5	101-3-I 702-60511	Screw, Bind Hd Machine +M2.6X5
6	101-3-1702-61211	Screw, Bind Hd Machine +M2.6X12
7	143-2-3404-09700	Protector
or	143-2-3404-I 0100	Protector
or	143-2-3404-I 1300	Protector
8	143-2-7804-00300	Master, Cam
9	112-3-I 302-50040	E-Ring, M2.5
10	143-2-6304-00700	Washer, 3.2X6X0.25
11	143-o-3404-01 002	Loading, Drive Complete
12	101-3-I 702-625 11	Screw, Bind Hd Machine +M2.6X25
13	101-3-I 702-60611	Screw, Bind Hd Machine+M2.6X6
14	4-5254-00240	Loading, Motor
or	4-5254-00241	Loading, Motor
15	101-3-I 303-00411	Screw, Pan Hd Machine ● tM3X4
16	143-2-6304-01500	Washer, Stopper 1.5X4X0.25
17	143-2-5504-02000	Pin, Worm
18	143-O-4904-00800	Worm Gear Assy
19	143-2-7504-00300	Belt, Loading
20	143-2-6304-00300	Washer, 2.1 X5X0.25
21	106-3-I 102-0001 1	Nut, M2
22	143-2-3404-06800	Bracket. Loading
23	101-3-I 302-01011	Screw, Pan Hd Machine +M2X10
24	4-2644-00043	Latch, Coil
25	143-o-51 04-01500	Rack Assy

Ref No	Part No.	Description
26	143-0-3404-01900	Bracket, Reel Assy
or	143-O-3404-02500	Bracket, Reel Assy
27	I 43-2-5804-02508	Screw, Pan Hd Tapping Del-Tite M2.6X8
28	143-2-6304-02900	Washer, 6X3.1 X0.3
or	143-2-6304-03000	Washer, 6X3.1 X0.4
or	143-2-6304-03100	Washer, 6X3.1 X0.5
29	143-O-41 04-00700	Reel Take Up Assy
or	143-O-41 04-00900	Reel Take Up Assy
30	1 43-O-41 04-00600	Reel Supply Assy
or	143-0-4104-00800	Reel Supply Assy
or	143-O-41 04-01000	Reel Supply Assy
31	143-2-6304-01800	Washer, Stopper 2.5X6X0.25
32	143-2-4904-01300	Gear, Loading Take Up
33	112-3-I 301-50040	E-Ring, MI .5
34	143-2-6304-00600	Washer, 2.1 X4X0.25
35	101-3-1302-6121 1	Screw, Pan Hd Machine +M2.6X12
36	143-2-6704-02400	Spring, Stopper
37	143-2-6704-02600	Cap, Stopper
38	143-O-5 104-01600	Main Plate Assy
39	143-2-7804-00200	Actuator, Cam
40	143-2-6604-04600	Spring, Actuator Cam
41	o-4064-00282	Stage Switch Assy
42	101-3-I 302-00811	Screw, Pan Hd Machine +M2X8
43	143-o-51 04-02400	Arm, Idler Control Complete
44	143-2-6604-04100	Spring, Arm Control
45	143-2-6704-03700	Spring, Earth

NOTE: Parts order must contain Model Number, Part Number and Description.

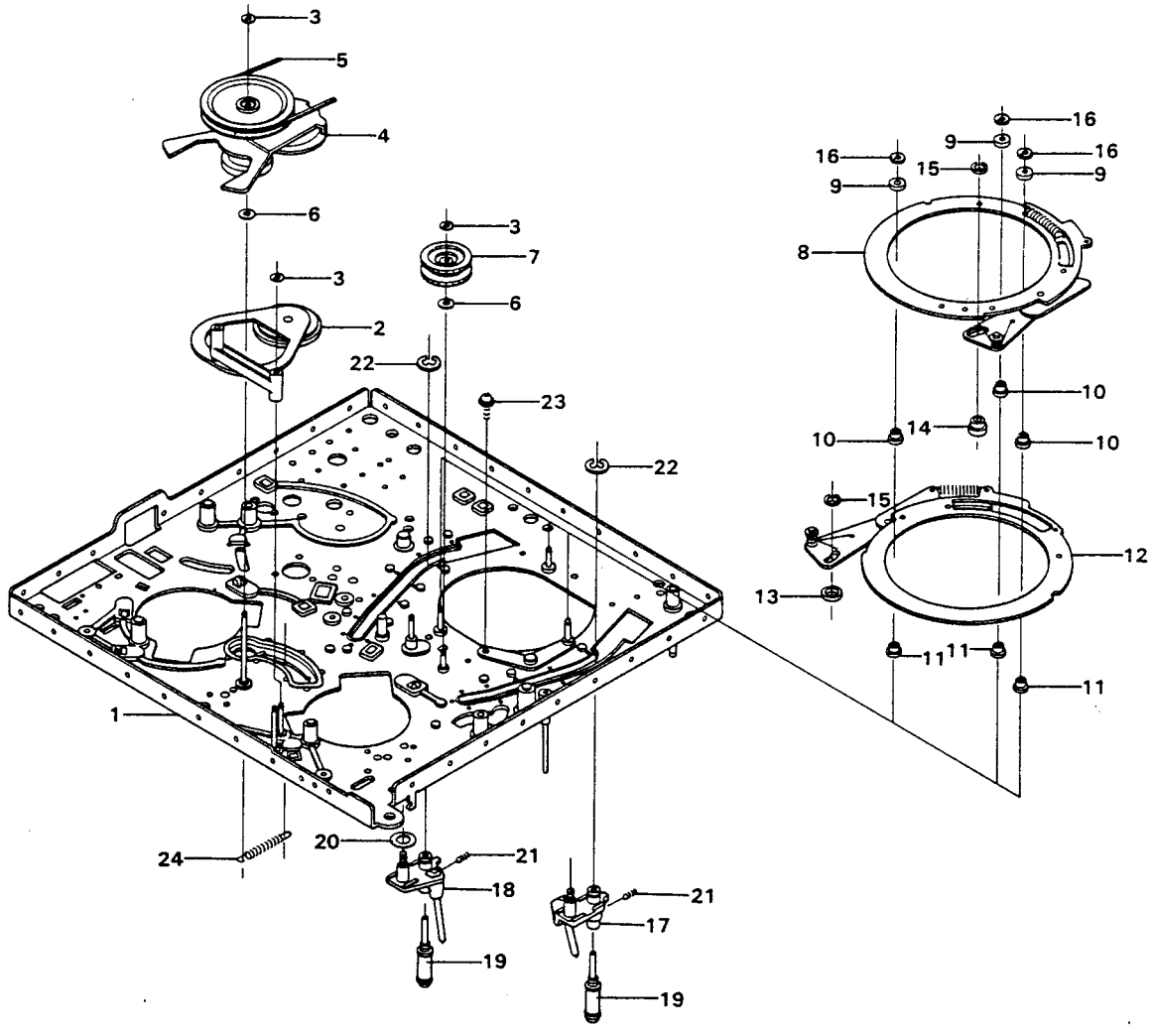


CHASSIS PARTS (5)

Ref No	Part No.	Description
1	143-0-3104-00301	Chassis Assy
or	143-0-3104-00401	Chassis Assy
or	143-0-3104-00501	Chassis Assy
2	143-0-4204-00400	Idler, Complete
3	143-2-6304-01500	Washer, Stopper 1.5X4X0.25
4	143-0-4904-00900	Gear, Idler Complete
5	143-2-7504-00400	Belt, Drive
or	143-2-7504-00600	Belt, Drive
6	143-2-6304-00600	Washer, 2.1X4X0.25
7	143-2-4904-00800	Gear, Loading Supply
8	143-0-4904-00700	Ring, Loading Supply Complete
9	143-2-4804-01200	Roller-Lower
10	143-2-4804-01100	Roller-Center
11	143-2-4804-01000	Roller-Upper

Ref No	Part No.	Description
12	143-0-4904-00500	Ring Loading Take Up Complete
13	143-2-5604-02600	Spacer, Take Up
14	143-2-5604-02500	Spacer, Supply
15	112-3-1302-00040	E-Ring, M2.0
16	143-2-6304-01600	Washer, Stopper 1.6X5X0.5
17	143-0-5104-01000	Base, Guide Roller Supply Assy
or	143-0-5104-02900	Base, Guide Roller Supply Assy
18	143-0-5104-00900	Base, Guide Roller Take Up Assy
19	143-0-7704-00400	Guide Roller Assy
or	143-0-7704-00600	Guide Roller Assy
20	143-2-4704-01500	Washer, Adjust
21	115-3-3502-00486	Screw, Cone Type Hex +M2X4
22	112-3-1304-00040	E-Ring, M4.0
23	143-2-5804-02205	Screw, Pan Hd Machine +M2.6X5
24	143-2-6604-04500	Spring, Idler

NOTE: Parts order must contain Model Number, Part Number and Description.



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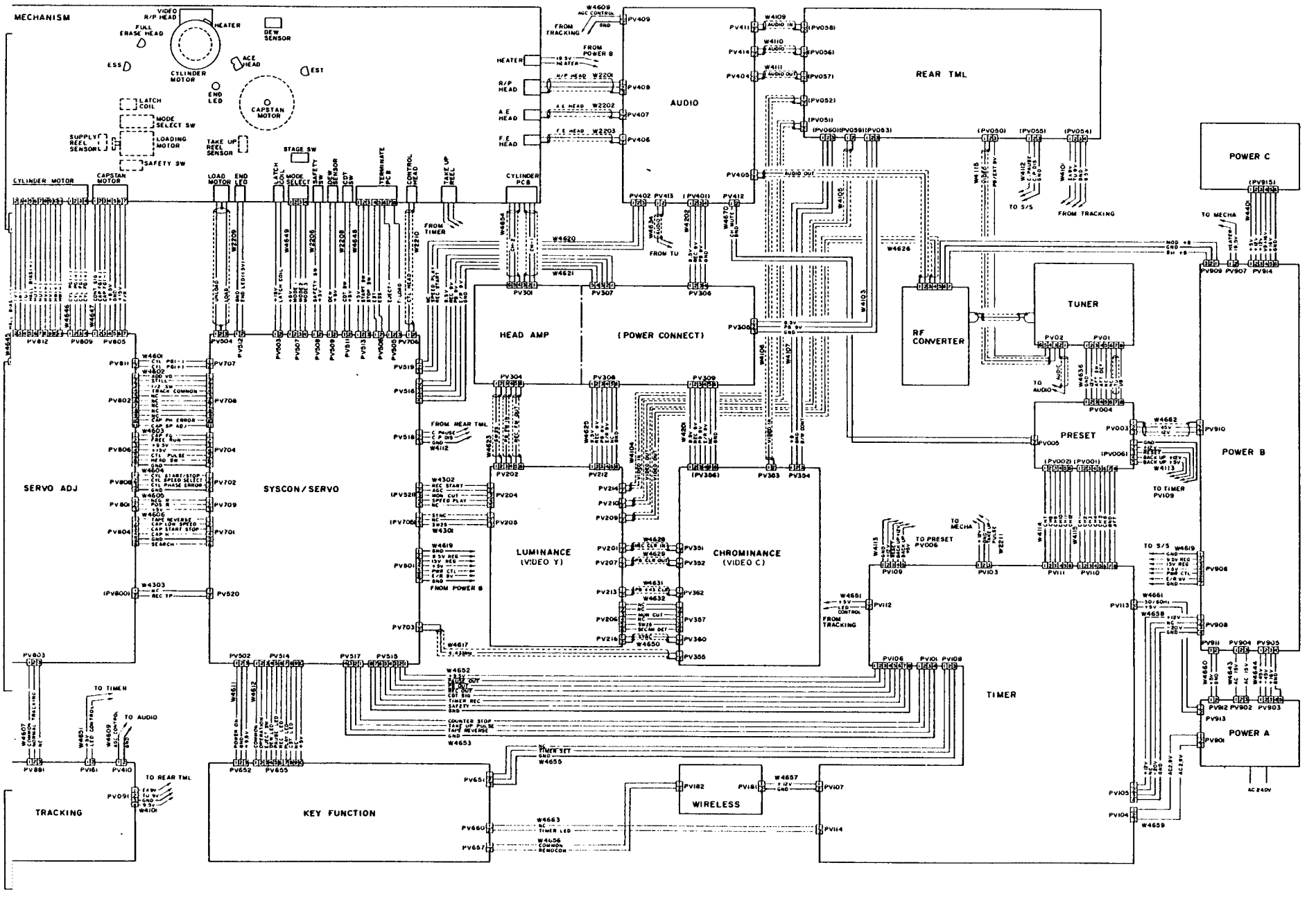
PRODUCTION SAFETY NOTICE

PRODUCT SAFETY SHOULD BE CONSIDERED WHEN A COMPONENT REPLACEMENT IS MADE IN ANY AREA OF A UNIT. COMPONENTS INDICATED BY THE SYMBOL ⚠ IN THIS SCHEMATIC DIAGRAM SHOW COMPONENTS WHOSE VALUE HAVE SPECIAL SIGNIFICANCE TO PRODUCT SAFETY. IT IS PARTICULARLY RCOMMENDED THAT ONLY PARTS SPECIFIED ON THE ATTACHED PARTS LIST BE USED FOR COMPONENT REPLACEMENT DESIGNATED BY THE SYMBOL.

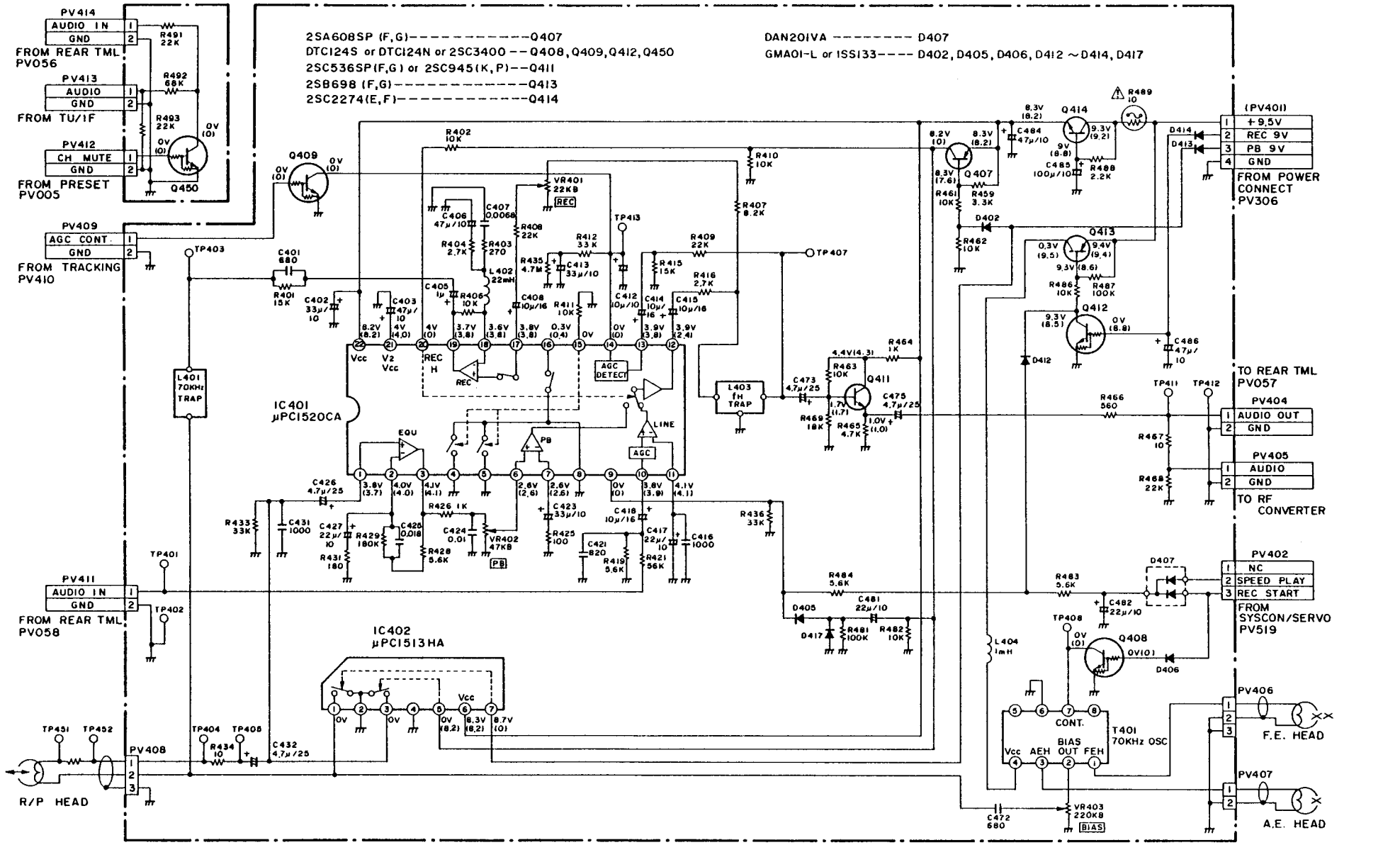
NOTES:

1. All resistance values in "OHMS" unless otherwise noted. (K=1,000 M=1,000,000)
2. All inductance values in "mH" unless otherwise noted. μ=micro henry.
3. Unless otherwise noted in schematic diagram, all Capacitors less than 1 are expressed in mfd, and the values larger than 1 are in pF.
4. Voltage reading may vary $\pm$20%
5. This is a fundamental circuit diagram. Some production changes may be made without revision of the diagram.

OVER ALL WIRING DIAGRAM

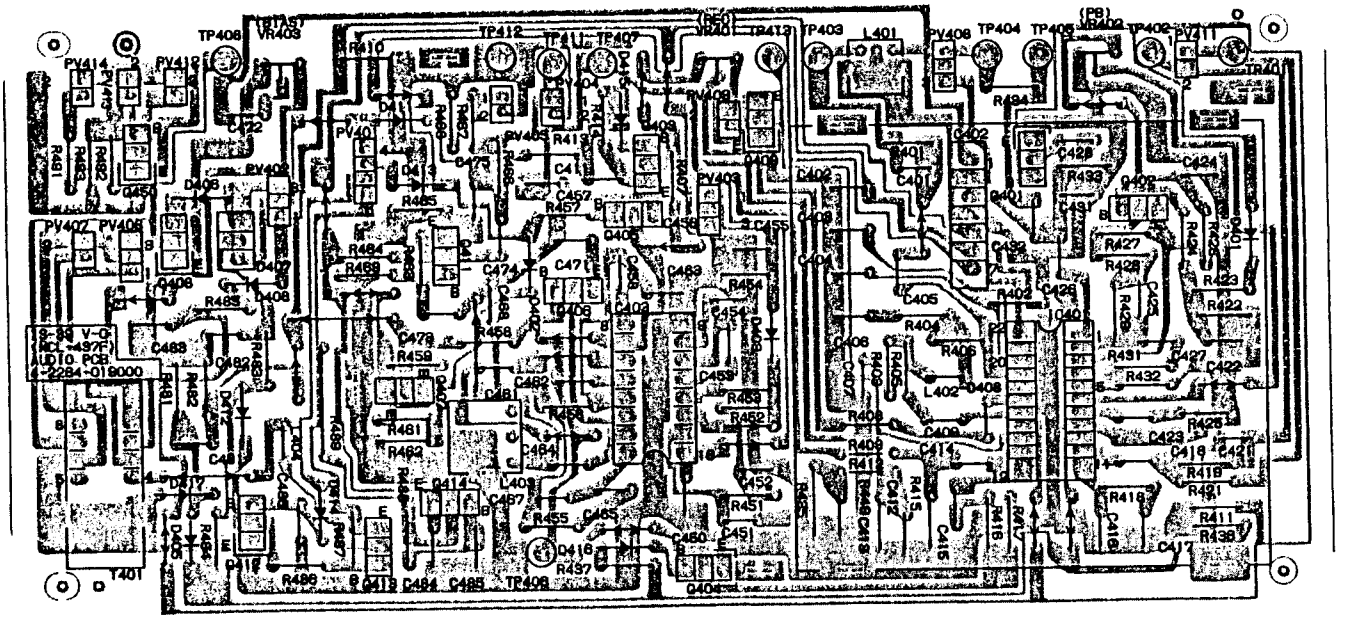


AUDIO CIRCUIT DIAGRAM

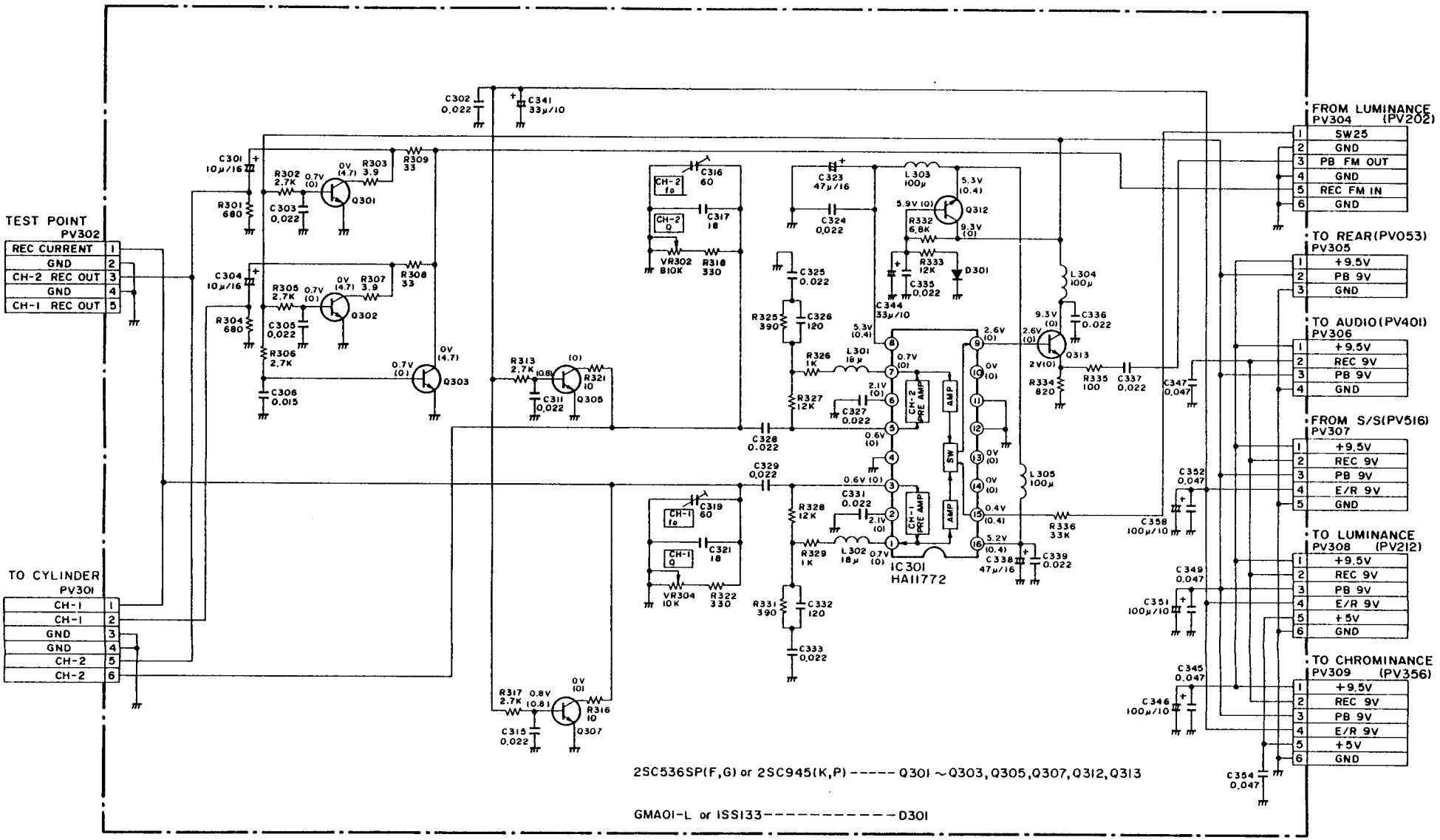


NOTE:
All voltage are in PLAY mode unless otherwise noted.
( )=RECORD mode only

AUDIO CIRCUIT P.C.B.

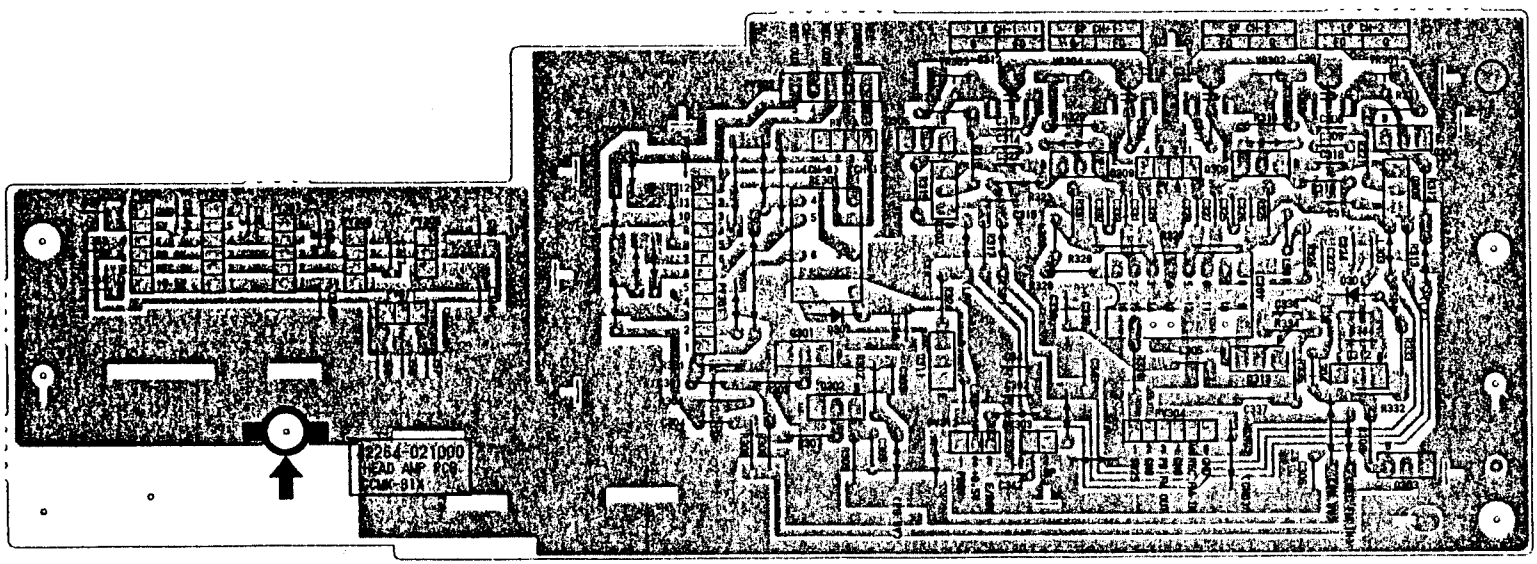


HEAD AMP CIRCUIT DIAGRAM

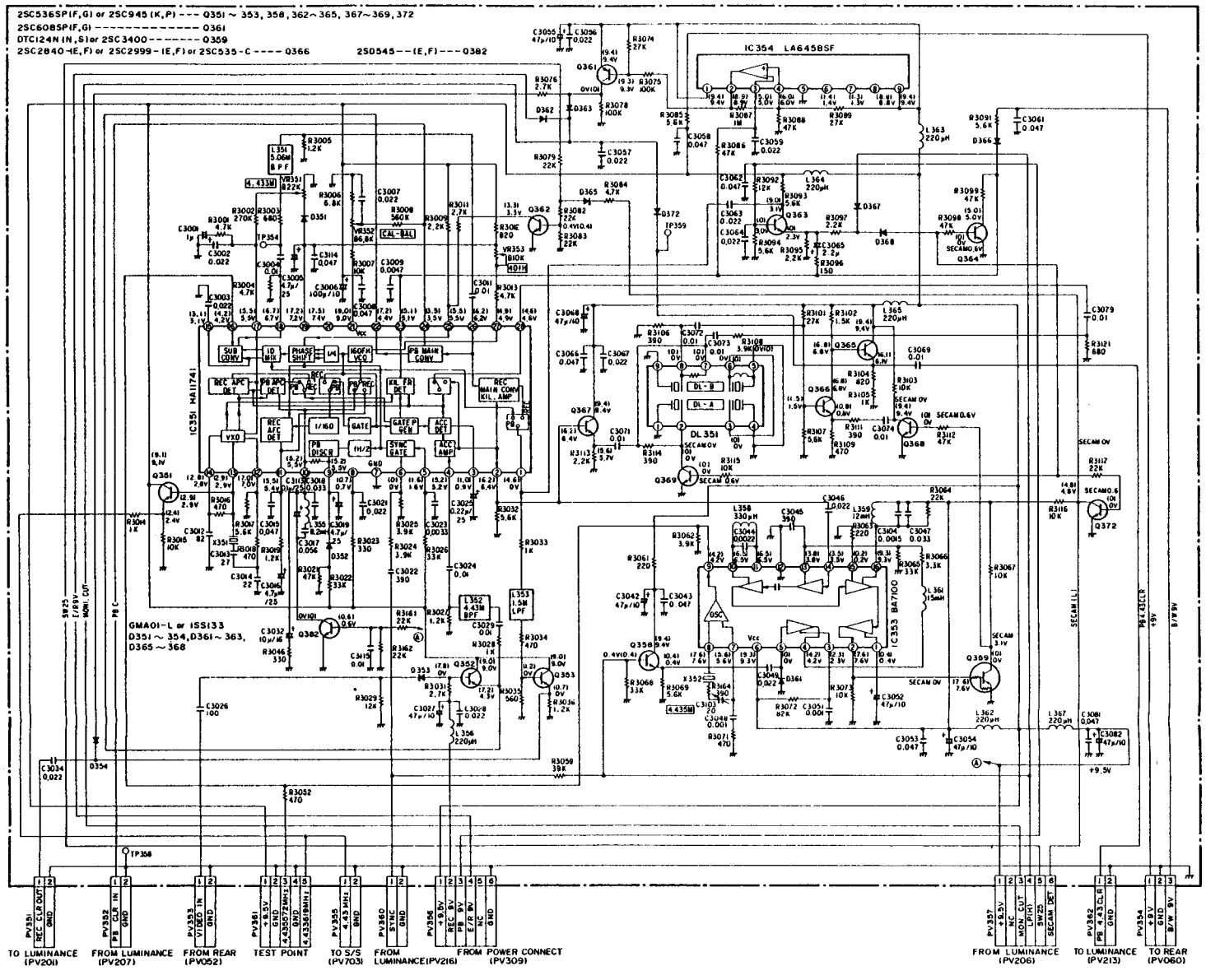


NOTE:
All voltage are in PLAY mode unless otherwise noted.
( )=RECORD mode only

HEAD AMP CIRCUIT P.C.B.

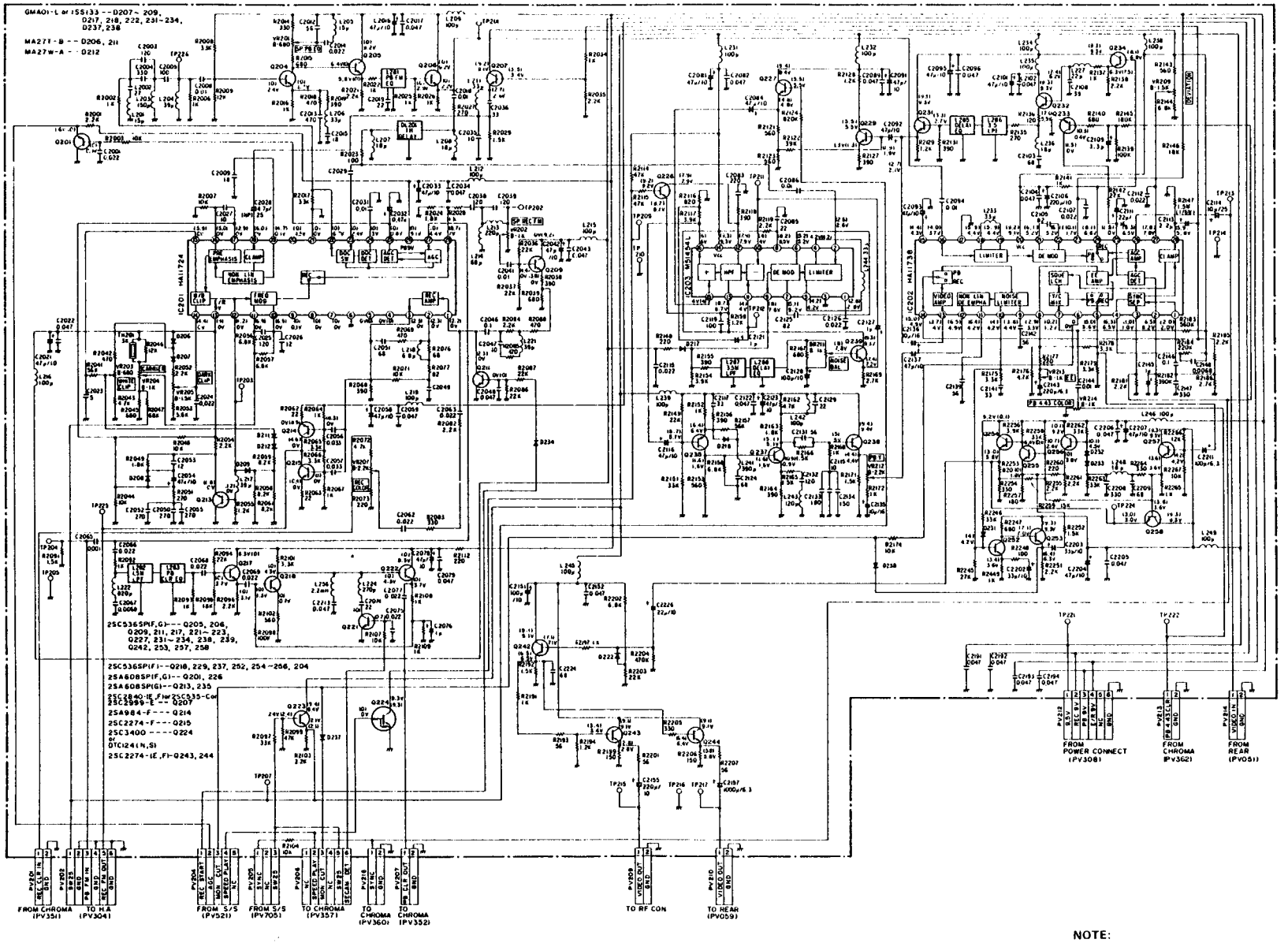


CHROMINANCE CIRCUIT DIAGRAM



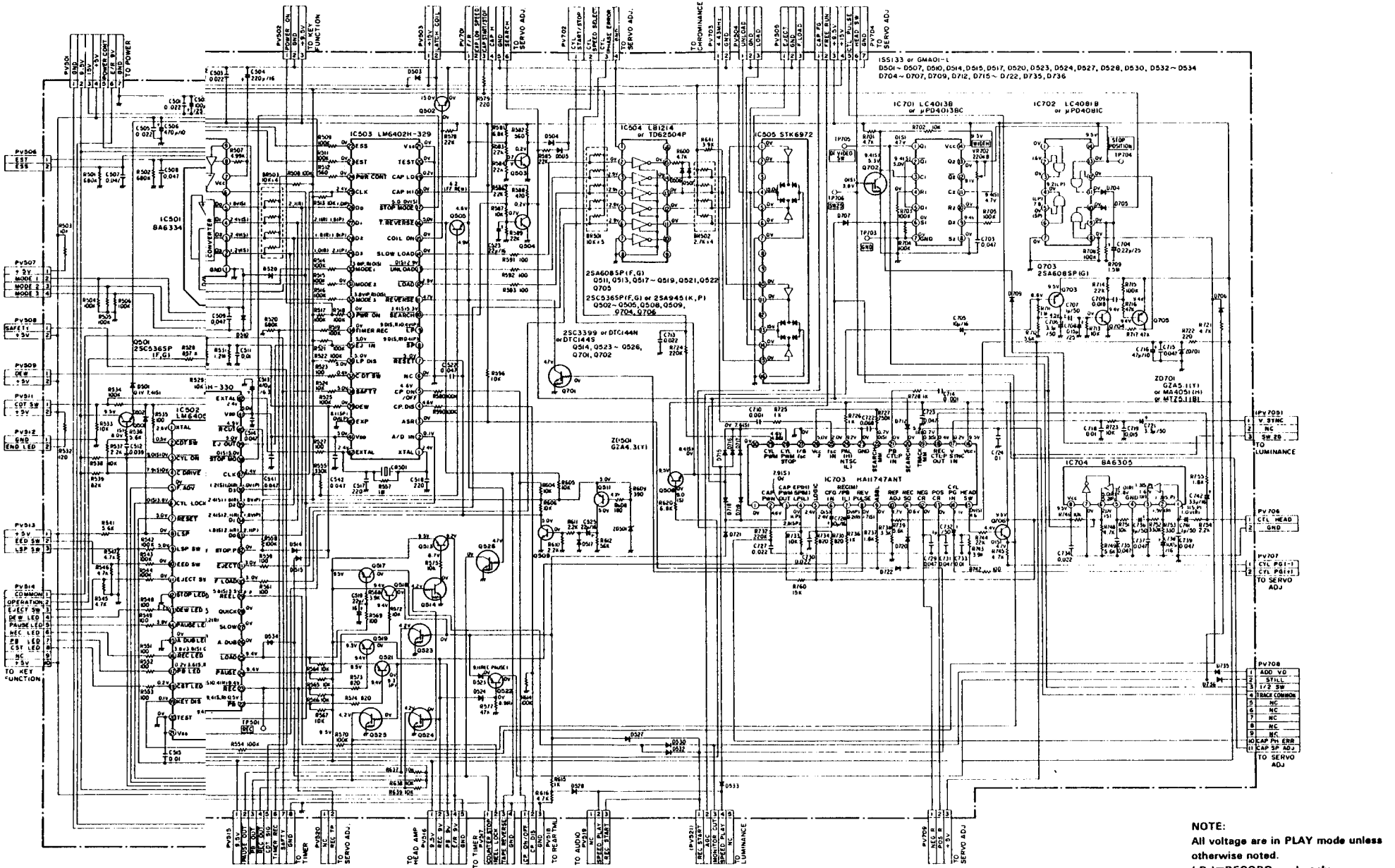
NOTE:
All voltage are in PLAY mode unless otherwise noted.
( )=RECORD mode only

LUMINANCE CIRCUIT DIAGRAM



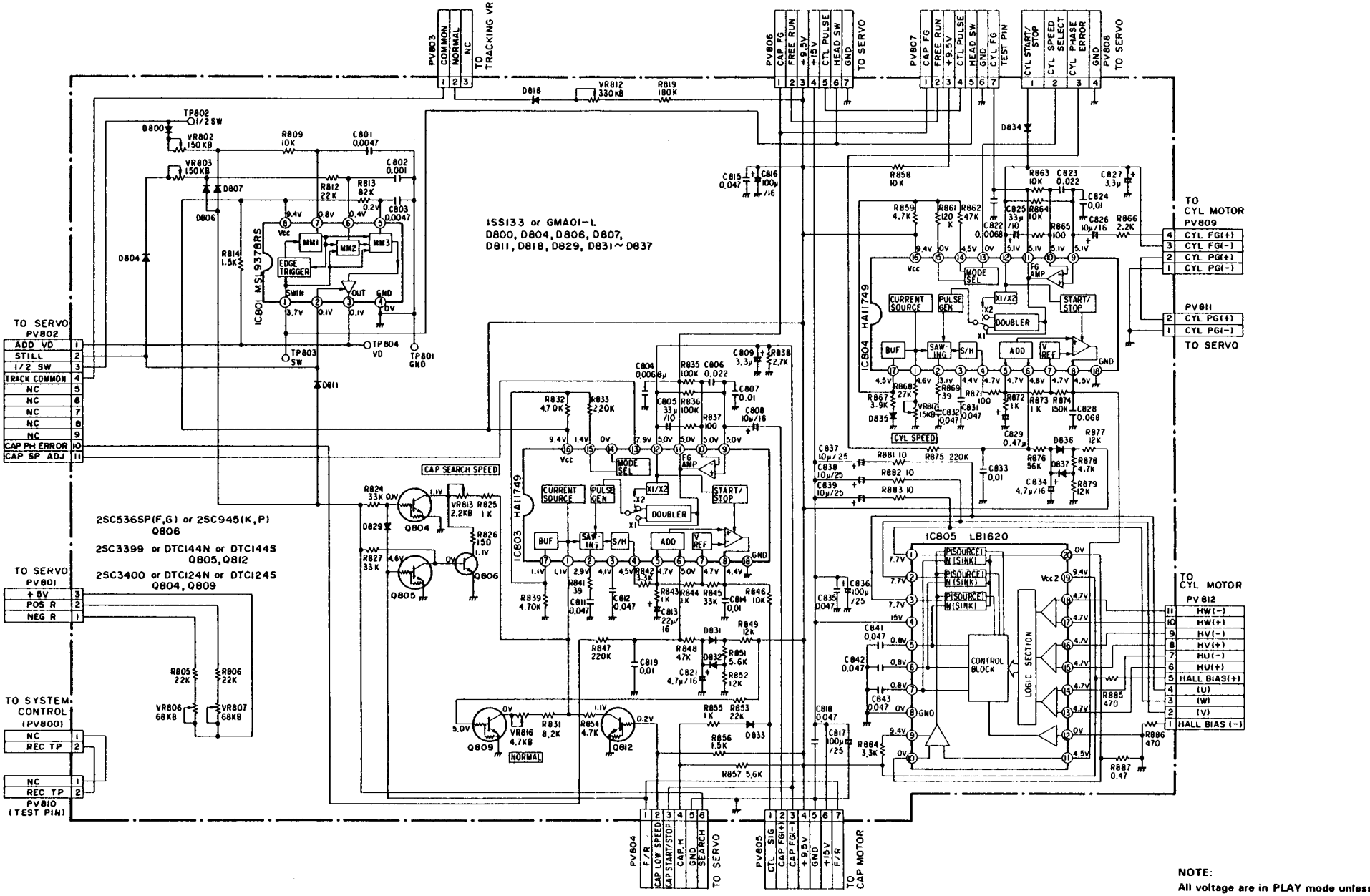
NOTE:
All voltage are in PLAY mode unless otherwise noted.
( )=RECORD mode only

SYSTEM CONTROL SERVO CIRCUIT DIAGRAM



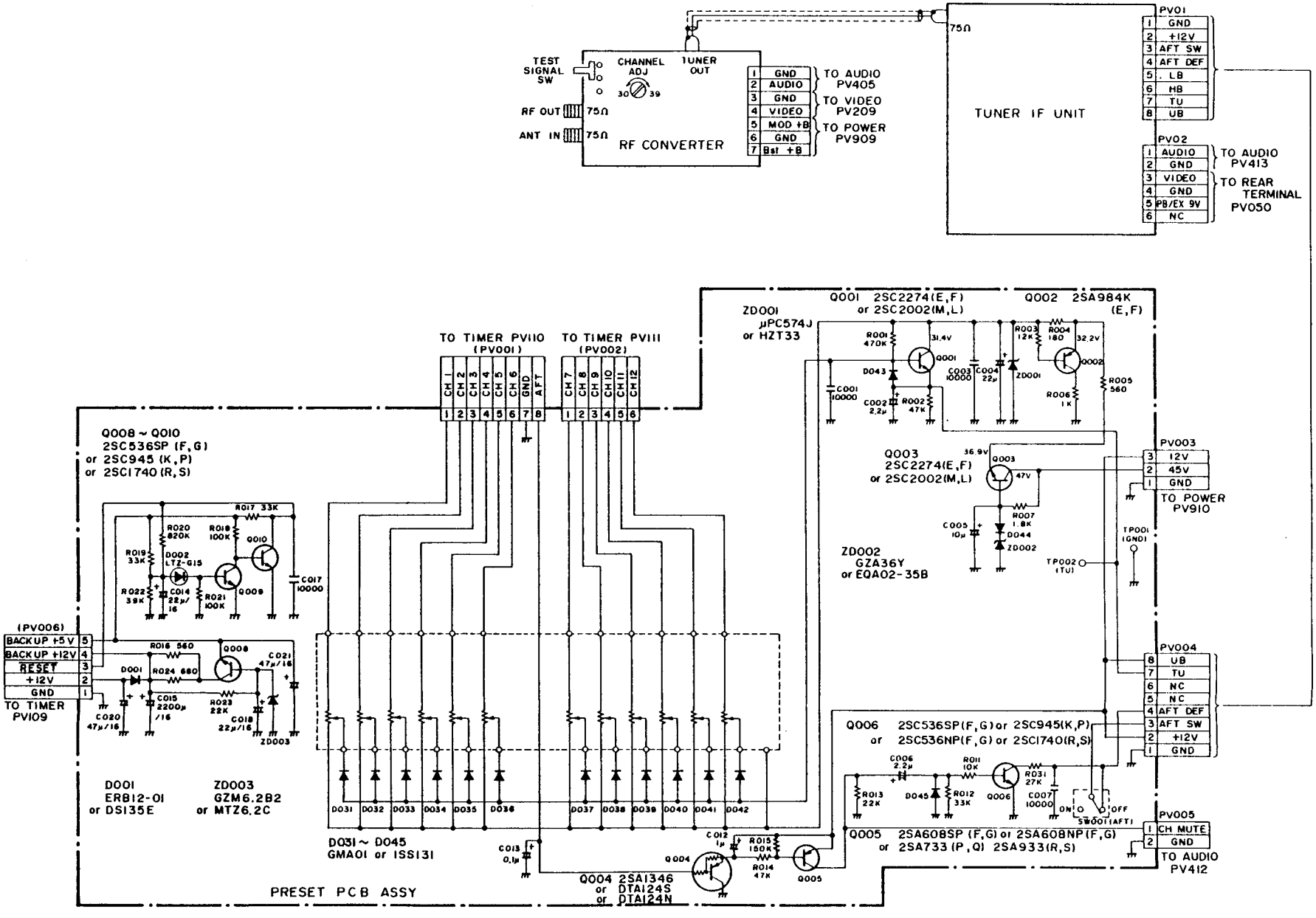
NOTE:
All voltage are in PLAY mode unless otherwise noted.
(R)=RECORD mode only
(S)=STOP mode only
(P)=PULSE signal

SERVO ADJUST CIRCUIT DIAGRAM

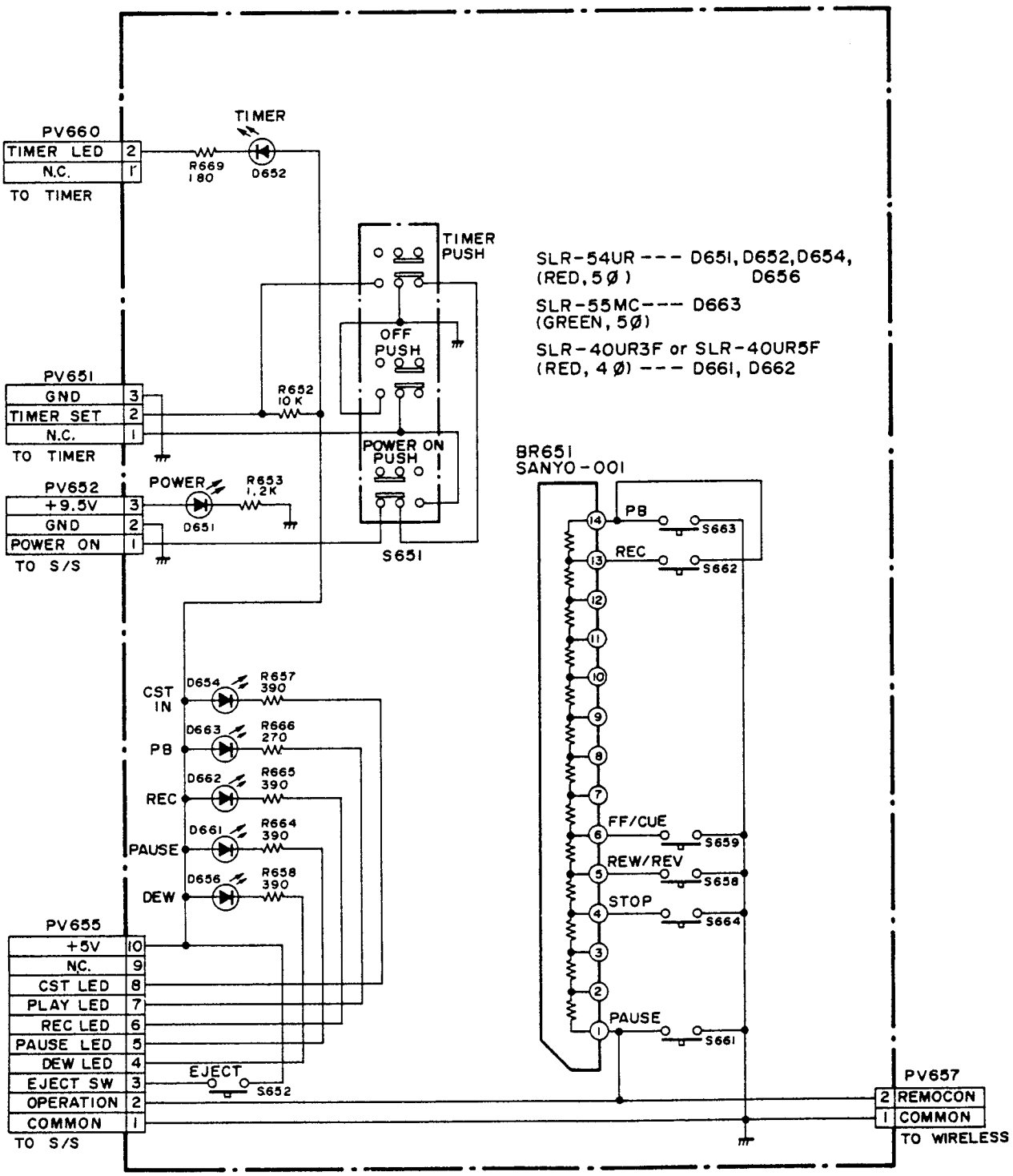


NOTE:
All voltage are in PLAY mode unless otherwise noted.
(S)=STOP mode only

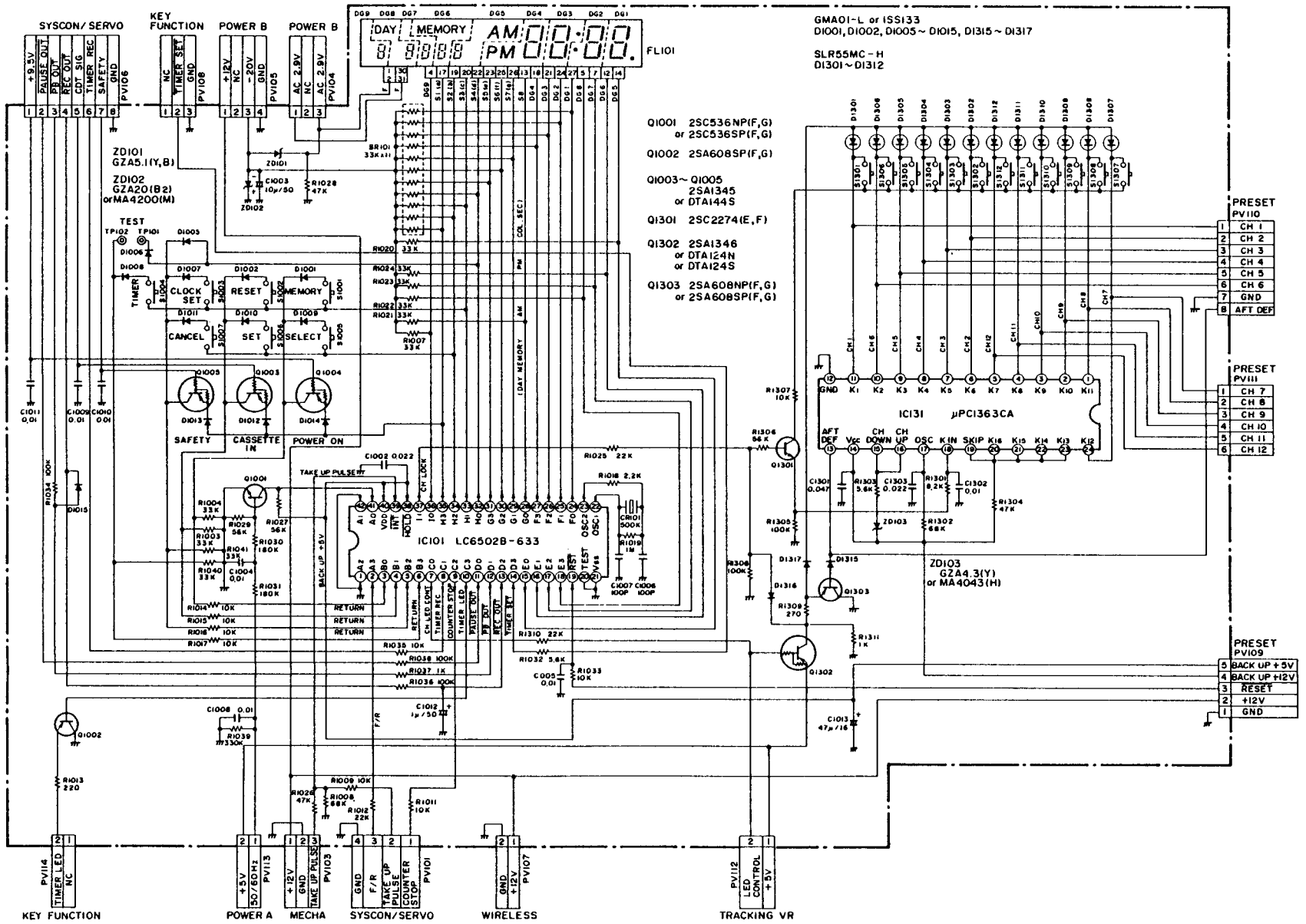
TUNER RF CONVERTER CIRCUIT DIAGRAM



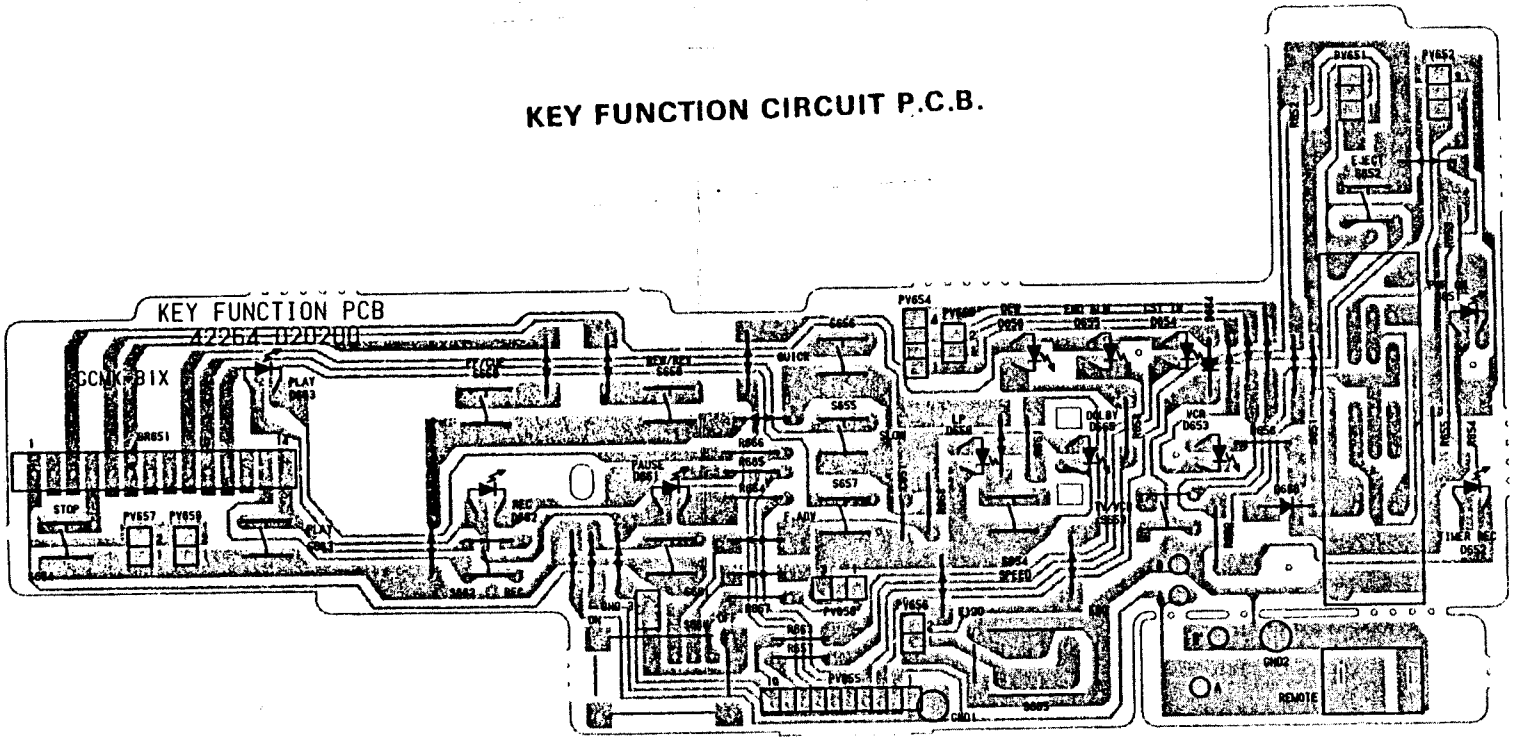
KEY FUNCTION CIRCUIT DIAGRAM



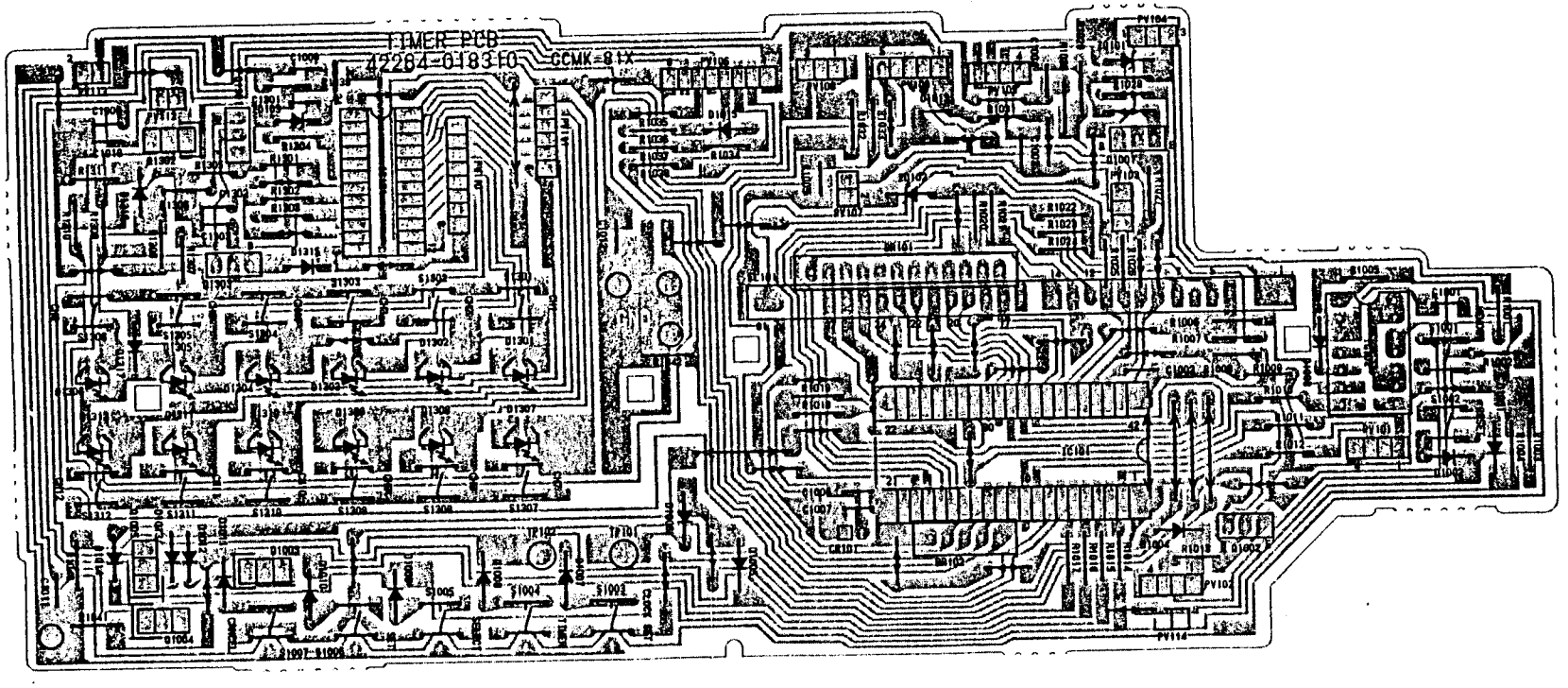
TIMER CIRCUIT DIAGRAM



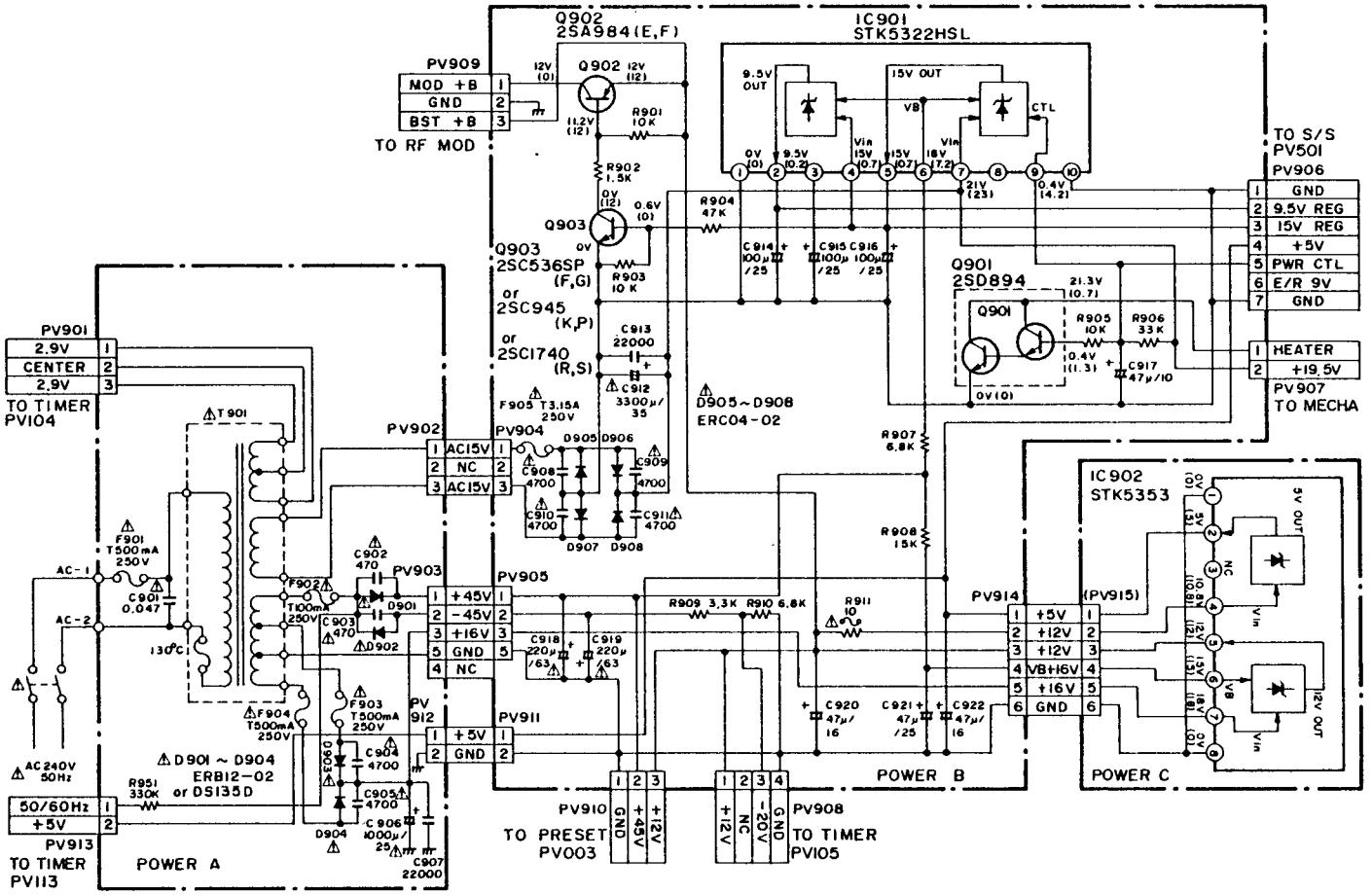
KEY FUNCTION CIRCUIT P.C.B.



TIMER CIRCUIT P.C.B.



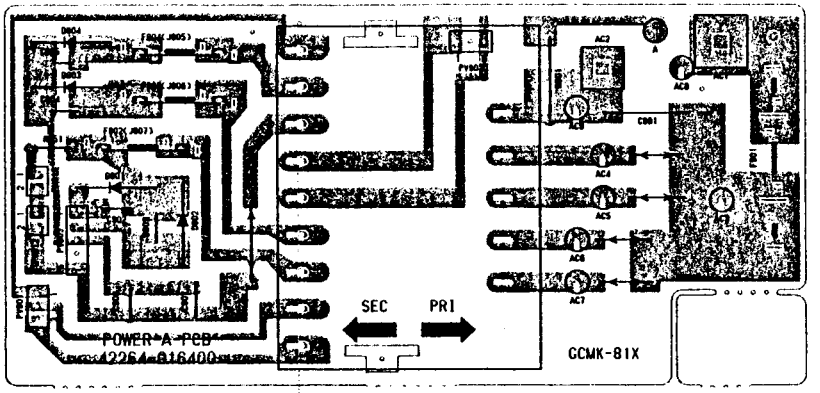
POWER CIRCUIT DIAGRAM



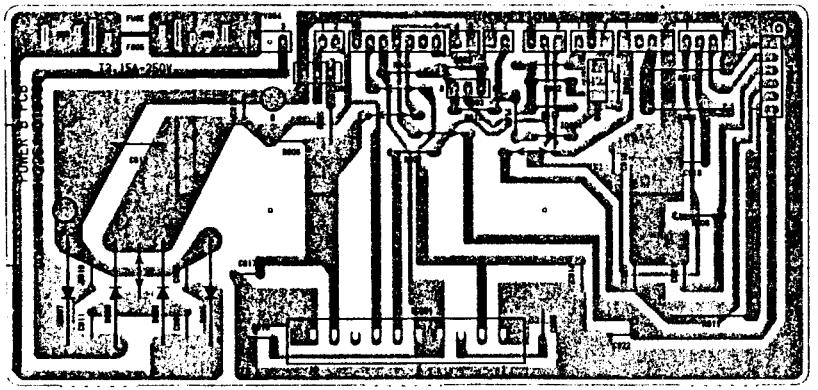
NOTES:
All voltage are in PLAY, RECORD and STOP mode unless otherwise noted.
( )=POWER OFF mode only

POWER A. B. AND C. CIRCUIT P.C.B.

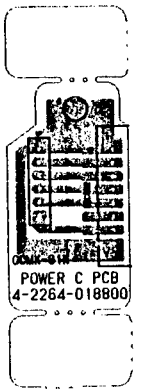
POWER A CIRCUIT P.C.B.



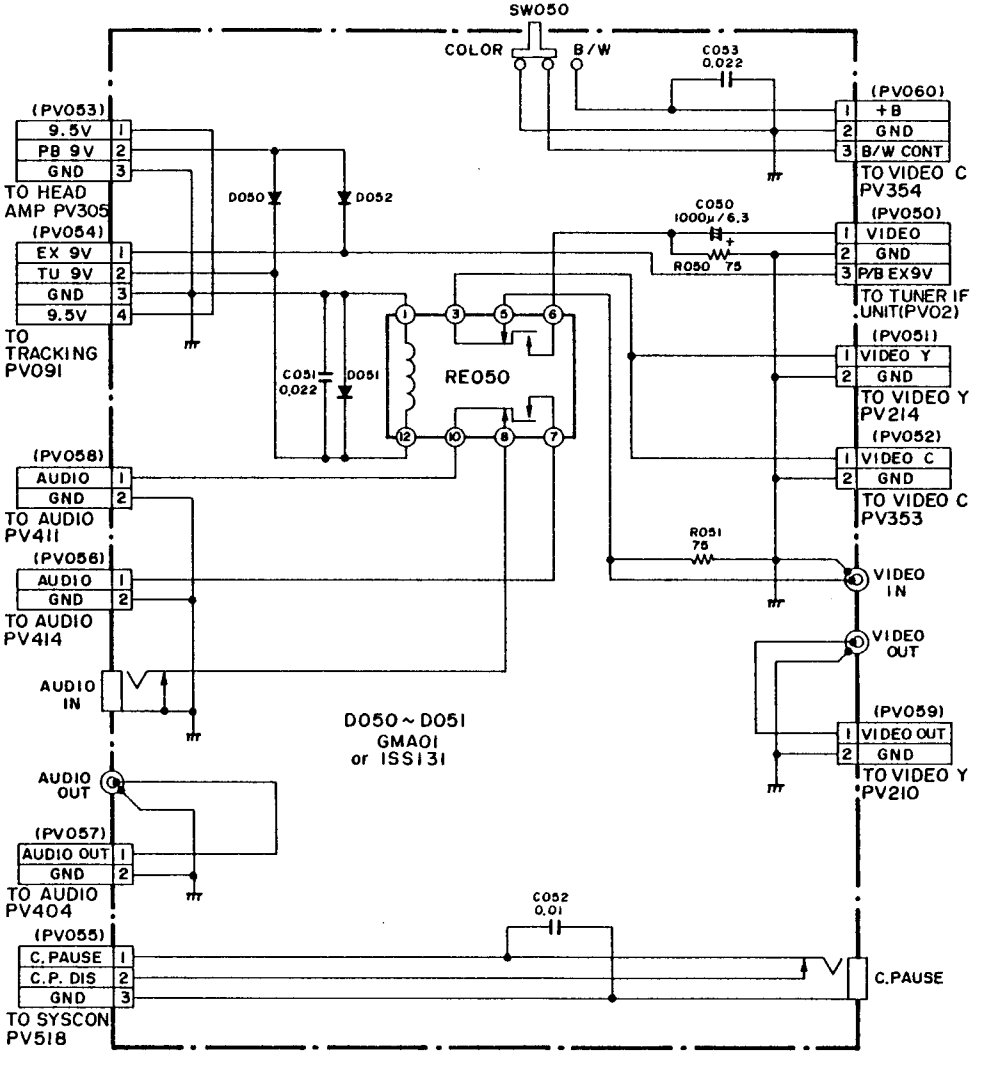
POWER B CIRCUIT P.C.B.



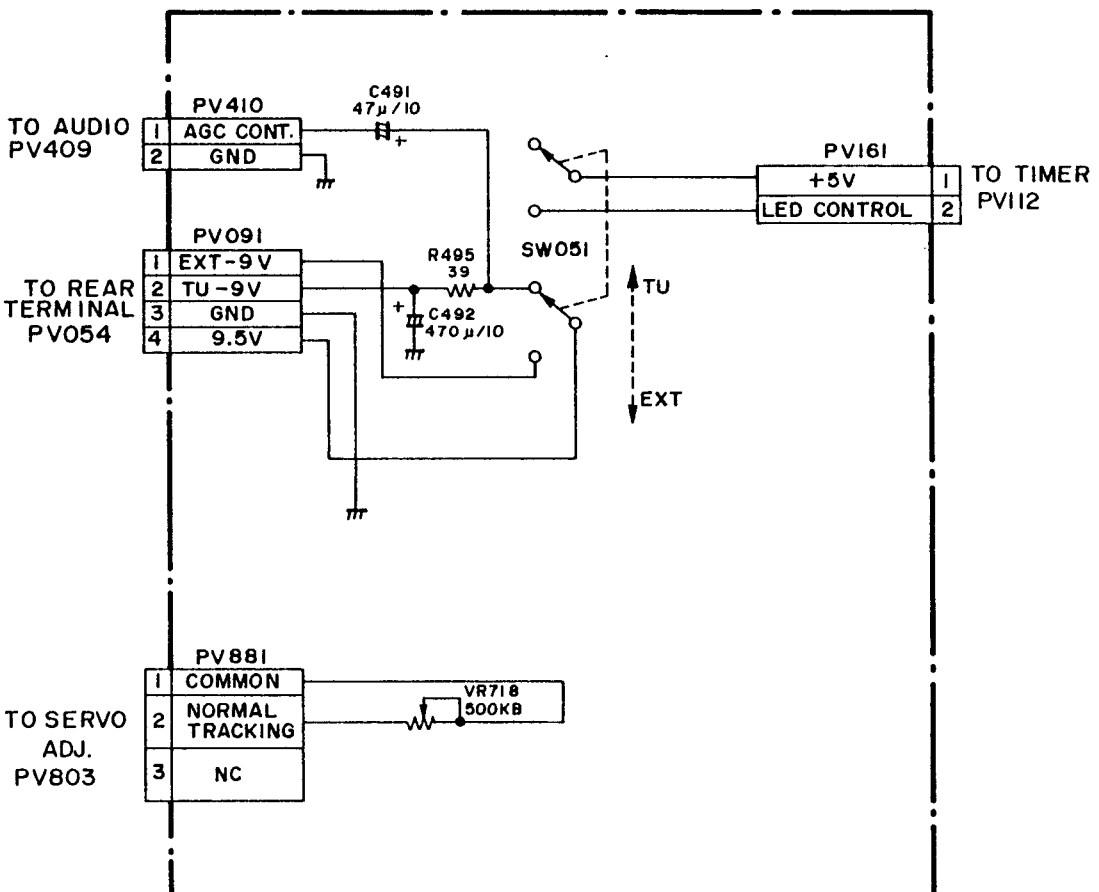
POWER C CIRCUIT P.C.B.



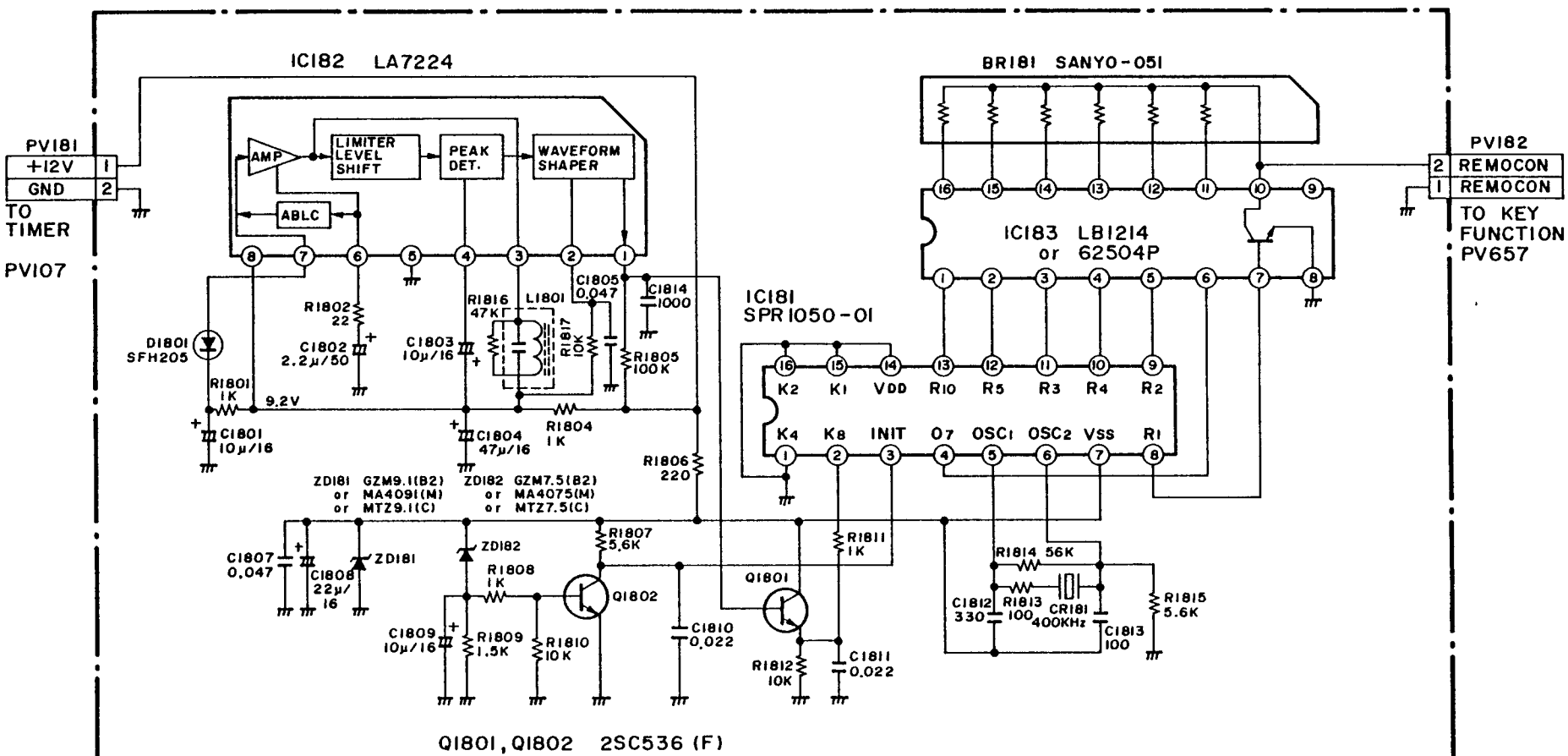
REAR TERMINAL CIRCUIT DIAGRAM



TRACKING VR CIRCUIT DIAGRAM

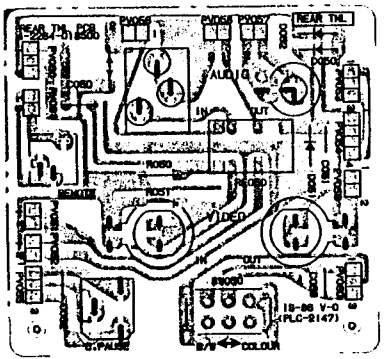


WIRELESS CIRCUIT DIAGRAM

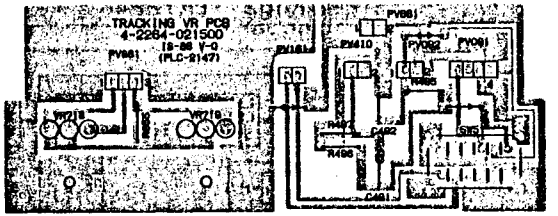


REAR TERMINAL. TRACKING VR. WIRELESS CIRCUIT P.C.B.

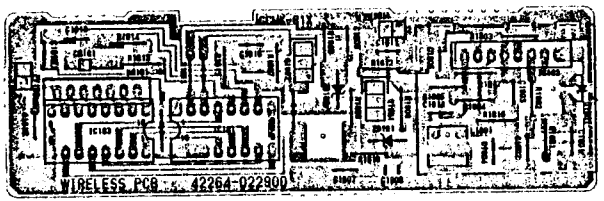
REAR TERMINAL CIRCUIT P.C.B.



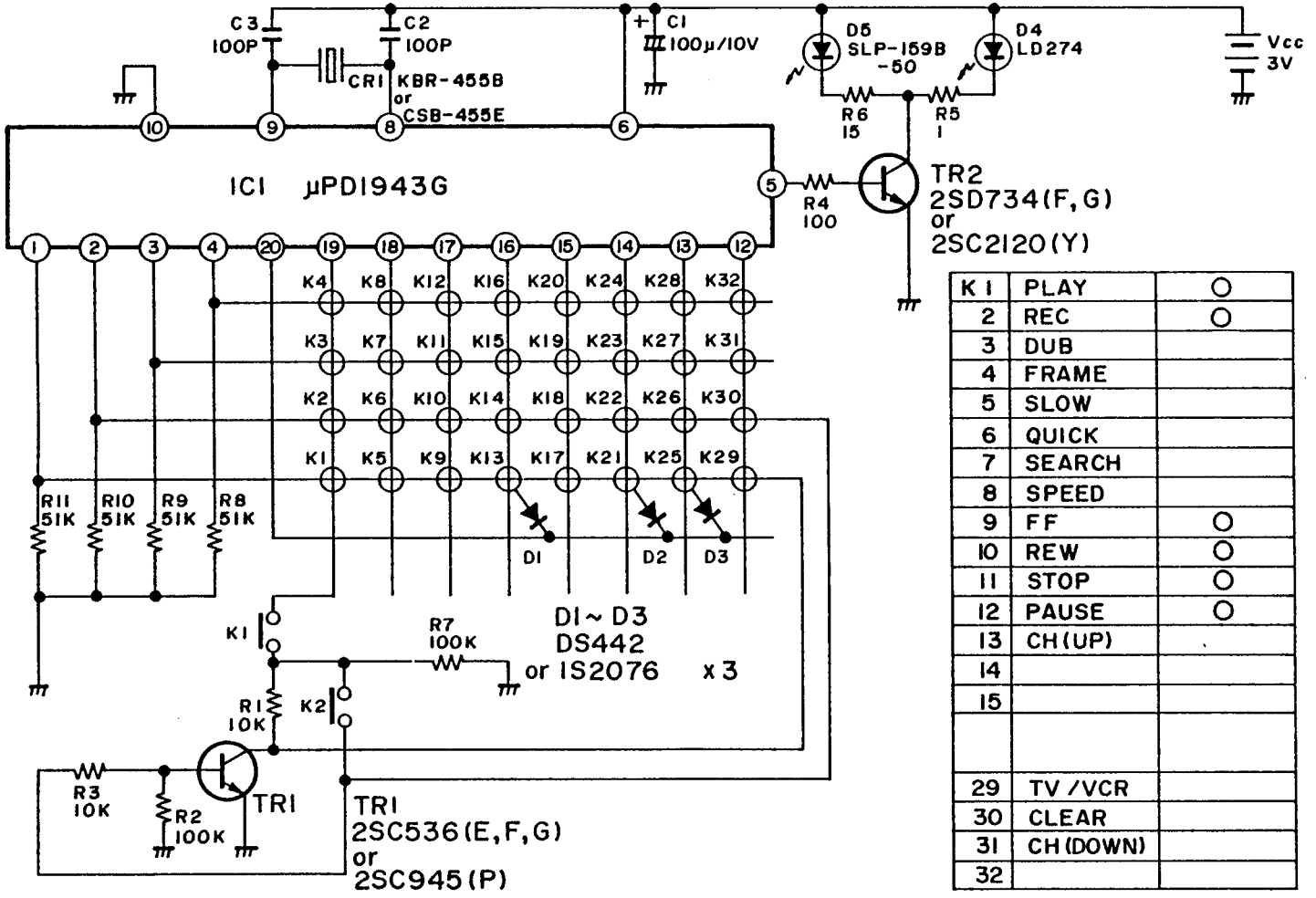
TRACKING VR CIRCUIT P.C.B.



WIRELESS CIRCUIT P.C.B.



REMOTE CONTROL CIRCUIT DIAGRAM



K1	PLAY	○
2	REC	○
3	DUB	
4	FRAME	
5	SLOW	
6	QUICK	
7	SEARCH	
8	SPEED	
9	FF	○
10	REW	○
11	STOP	○
12	PAUSE	○
13	CH(UP)	
14		
15		
29	TV/VCR	
30	CLEAR	
31	CH(DOWN)	
32		

TERMINAL VIEW

2SD894

2SA733 2SC535 DTA124N
2SA933 2SC945 DTC124N
2SA984 2SC2002 DTC144N
2SA1345 2SC2274
2SA1346 2SC3400
2SB698 2SD645

2SA608SP 2SC3399
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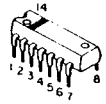
2SC536SP

MSL9378RS



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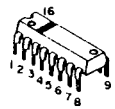
LC4081B
μPD4013BC
μPD4081C



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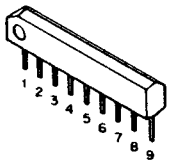

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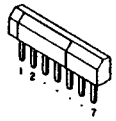

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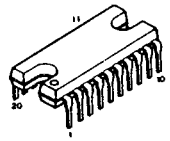

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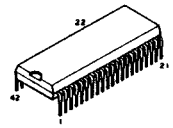
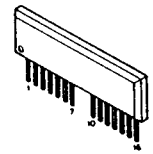
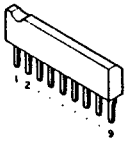


LC6502B-633
LM6402H-329
LM6405H-330



STK6972



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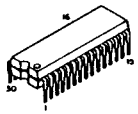

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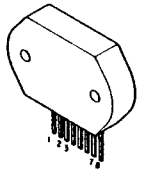

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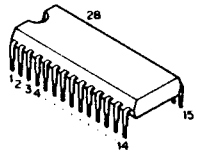
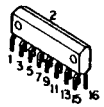


HA11724
HA11738
HA11741



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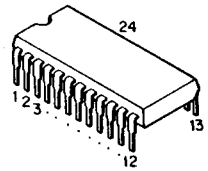

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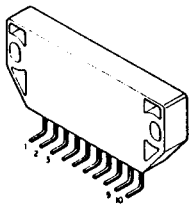

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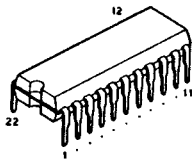

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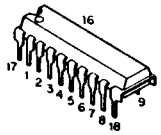

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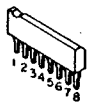

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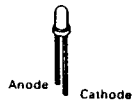
DAN201VA



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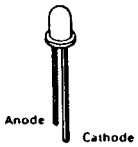
SLR40UR-5F



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SLR55MC
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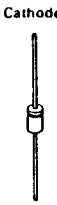
DS135D
DS135E
ERB12-01
ERB12-02



ERC04-02

EQA03-35B GMA01 MA4091(M)
GZA4.3Y GMA01-L MA4075(M)
GZA5.1Y HZT33 MTZ6.2(C)
GZA36Y MA27TB MTZ7.5(C)
GZM6.2(B2) MA27WA MTZ9.1(C)
GZM7.5(B2) MA4043(H) LTZG15
GZM9.1(B2) MA4051(H) 1SS131
1SS133

NOTE:
E: Emitter C: Collector B: Base

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